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Final Technical Report
June 1978

CHARACTERIZATION OF COMPLEX MICROPROCESSORS & SUPPORT CHIPS

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The objective of this effort was to develop high test confidence level functional tests and parametric tests for selected microprocessors and microprocessor support devices; and then generate MIL-M-38510 slash sheets for them which conformed to military standards. This included worst case test situations, critical timing and generation of new test procedures where present or accepted methods no longer apply. User and manufacturer comments made to microprocessor slash sheets/400 and /420 developed under a

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previous contract* were reviewed with device manufacturers and changes were made to the slash sheets where necessary. Military qualification of these devices was supported also as it applied to the slash sheet test methods and procedures.

*Report RADC-TR-77-91 March 77

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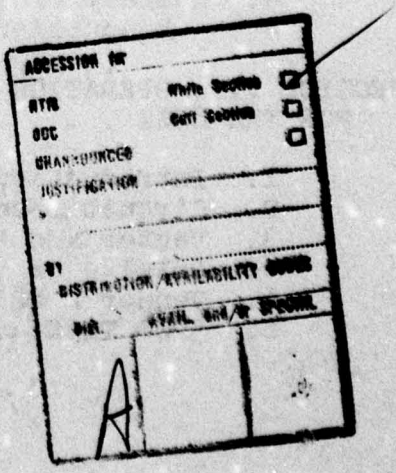
PREFACE

This Final Report was prepared by General Electric Ordnance Systems, 100 Plastics Avenue, Pittsfield, Massachusetts, for Rome Air Development Center, Griffiss Air Force Base, New York, under contract F30602-77-C-0012.
It covers the period December 1976 to January 1978. Mr. Regis C. Hilow, RBRM, was the RADC Project Engineer.

The work on this project was performed by the Electronic Circuits Engineering Operation and Components Engineering Unit. Project responsibility was held by Mr. Thomas M. Ostrowski of Circuit Design Engineering. Key individuals who made significant contributions to this report were Messrs. Barney Hajduk, Richard English, Larry Roller, Lawrence DeLuca, Winston Taylor, James Schwehr, David O'Connor, David Prystasz, and Clarence Carey.



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EVALUATION

The prime objective of this study was to electrically characterize semiconductor microprocessors and their support devices over the defined military temperature range of -55°C to +125°C. This included assurance that the devices studied met established military standards, were technically accurate and electrically complete.

This effort concentrated on final vendor negotiations of the 8080A and 6800 microprocessor detail M38510 specifications. This resulted in the JAN qualification of the Intel Corp as a source for the 8080A and Motorola Semiconductor as a source for the 6800. Major emphasis in this program was also placed on electrically characterizing the 2900 bit-slice microprocessor and its support devices. Details of this work are contained in this report. Finally, the general problem area of testing a tristate output was evaluated resulting in an effective load network applicable to all tristate outputs. This network replaces several relays and other components thus saving the vendor test cost, time and providing a more reliable test panel.

RADC, as Preparing Activity of MIL-M-38510, General Specification for Microcircuits, is responsible for managing the development and preparation of detail slash sheets for this specification. This study and future studies will be expanded in the microprocessor area and accelerated to provide DOD system builders with state-of-the-art devices specified to meet military environmental requirements.

REGIS C. HILOW
Project Engineer

SECTION I

SUMMARY

This report details a gate-level functional analysis performed on a microprocessor and microprocessor support devices. These results were used in the generation of MIL-M-38510 slash sheets (not included here). The characterized devices are listed below.

The microprocessor test philosophy used for this effort was established on a previous contract with RADC and was reported in Report RADC-TR-77-91, March 1977. This philosophy was further developed and presented herein as a "Procedure For LSI Functional Test Development". During that previous effort two microprocessors, 6800 and 8080A, were characterized. The qualification of these devices occurred during this contract period, and the follow-on test development is reported here also.

The test development and qualification that occurred during this contract showed that new loading philosophies should be considered. A section of this report is devoted to this subject.

Characterized Devices

2901A Four-bit microprocessor slice

2918 Quad D-Register

2905, 06, 07, 15, 16, 17 Quad-bus Transceivers

8212 Eight-bit I/O port

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Section II

INTRODUCTION

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Objective and Background

This characterization was an extension of a similar effort (transacted on a previous contract for RADC (F-30602-74-0159) from which developed a test philosophy for microprocessors. This philosophy which was subsequently applied to the generation of the first Mil-M-38510 microprocessor slash sheets. Additional microprocessors were identified for characterization on this contract on the basis of military needs. These additional items included other device technologies (CMOS and bipolar) and types of processors (fixed instruction vs. bit blice). In order to provide the special purpose complimentary functions that most processors require, support devices were also identified for characterization.

This report includes detailed functional block level analyses of functional tests performed on the 2901A 4-bit slice central processing unit (/440) along with gate level analysis on the following microprocessor (μp) support chips: 2918 quad D register (/442); 2915, 2916, 2917, 2905, 2906, 2907-quad bus transceivers (/441) and the 8212-8-Bit I/O port (/421). Included with the support chip analyses are the functional tests that were developed and the functional test programs written for the Tetronix 3260 automatic tester. These programs were used to verify device functional test operation and were devised to be compatible with the capabilities of RADC's automatic tester.

During this characterization effort, qualification of both the 6800 and the 8080A (characterized on the previous contract) was in progress. These particular slash sheet tests and their format introduced new concepts to the military slash sheets. Automatic testers were necessary and extensive dynamic functional testing was required. Some test difficulties were encountered during qualification of these devices which ultimately resulted in the refinement of some of the test concepts. Device test problems were also encountered which similarly affected the functional tests. A considerable coordinated effort was made with the processor manufacturers to arrive at practical solutions which would serve as models for similar future specifications. These problems and their solutions are discussed in detail in this report in Section III.

As the characterization progressed, the lack of a commonly accepted, simple, easily implemented tristate load was apparent. Since processors and their support chips are bus oriented, tristate leakage and propagation delay testing are a part of virtually all of the processor related slash sheets. Without standard loads and test methods there would not be a common means of comparison. Dynamic loading, in general, and tristate loading in particular were reviewed. A load is proposed in Section IV of this report for use in future slash sheets along with several variations which address particular test problems.

As a result of analyzing another type of processor (2901A-4 bit slice) and the various support chips indicated above, the previously developed µp test philosophy was tempered and expanded upon to become a general test development approach. This approach can be applied to any LSI device for functional test development. Section V of the report, "Procedure for LSI Functional Test Development," describes this test approach.

An amendment (#1) to this contract increased the scope and time period of the contract so that another final report will be issued in mid 1978. This report will contain similar information on additional microprocessors and support chips.

SECTION III
TEST DEVELOPMENT FOR MIL-M-38510/400 AND /420 DURING QUALIFICATION

The Mil-M-38510/400 and /420 were the first two slash sheets of their type ever attempted for monolithic devices of such great complexity. Out of necessity, many of the test approaches and methods used were innovative for the slash sheets and device complexity dictated for the first time that large automatic testers were necessary.

This section reports on the major changes made to the slash sheets as a result of device qualification. It is during qualification that test methods, procedures, and limits receive their greatest scrutiny by manufacturers. At this time one manufacturer is qualified to the /400 and another to /420.

Data Logging.

Taking parametric data on a microprocessor is a time-consuming procedure even with the aid of large automatic testers. During functional testing, devices are 100% checked on a go/no-go basis against parametric limits. This is readily accomplished on these machines.

This method does not provide useful data that can be used to gage parameter/process shifts or maturity of the device over a period of time. Provisions were therefore made in the slash sheet to take data during the qualification and period checks of these devices. When considering, the reiterative process used on some testers to "home in" on a data point, estimates of the length of time required to take data per device were prohibitive (4 hrs). Testers normally measure one parameter per one device pin at any time. In this regard a major change was made to facilitate data gathering.

The areas where savings in test time could be realized were the data and address buses. The change that was made allowed parallel "monitoring" of like bus pins" while data logging only the worst-case pin delay. The term "like bus pins" defines similar output buffer data paths and output buffer construction. It cannot be assumed that this would be the case for all 8 data or all 16 address outputs. For the Vendor E 6800 the address bus had to be split into two test groups because of construction dissimilarities. Without detailed knowledge of the construction of a device, these determinations cannot be made and should not be attempted.

A further reduction in test time was also obtained by data logging only the worst-case delay of eight possible delays on the address and data buses. Since substantially less data was now being taken, it was possible to monitor these outputs whenever they were relevant for the entire vector set, including replications for worst-case timing and voltages.

Previously vector numbers were assigned to each propagation delay; and it was here that a measurement was taken. These vectors were chosen primarily on the basis of the output being relevant. Predicting where in the program the worst-case occurred was not possible with available information. It should be mentioned that with proper schematics and layouts, this still would have been very difficult to predict.

Since the new test method requires sampling the full vector set along with replications for worst-case timing and voltage, the measurements not only reflect worst-case delays, but delays through all paths.

This general approach and the changes were agreed upon by major manufacturers of these microprocessors. Consequently, Table III and the table notes of /400 and /420 were rewritten.

In the future, where data gathering for complex devices like microprocessors becomes excessively time consuming, this approach is recommended for consideration.

Tristate Delay Measurements

Two problems were encountered which relate to tristate output measurements. The first occurs primarily on clocked complex combinatorial devices. It concerns the preloaded states of tristate output buffers.

In testing one particular microprocessor for t_{PHZ} (high level to tristate level), the tristate output buffers were preloaded with "zeros" as part of the functional test. Because a race condition existed between the occurrence of the tristate and the buffer switching to its preloaded state, the device tried to switch to a logic "0" level (from) a logic "1") instead of going into tristate. This condition was initiated

on a clock pulse. The tristate eventually dominates when the output buffer is disabled. However, a transient is introduced which can lead to an erroneous delay measurement. The measurement may be referenced to the transient instead of to the high impedance waveform. This can also occur for a t_{PLZ} measurement if the inputs to the output buffers are preloaded with "1's".

The solution is to preload the buffers with the logic levels that they would be switching from when going into tristate.

The second problem is related to the length of time it takes for R-C loaded outputs to reach the high impedance level. This time is highly dependent upon the ability of the resistive load to charge the load capacitance. Devices with low drive capability have large value resistive loads. Under these circumstances the propagation delay primarily consists of the charging of a load capacitance and can be an inordinately large number (600 to 800 nanoseconds (ns)).

A bus user wants to know when a bus has been released. If a bus has been released but has not had time to charge to some tristate level, the next user can drive it to the desired level. For critical timing conditions, if a 600-nanosecond delay consists of 100 ns of release time, the next user can take charge of the bus 500 ns sooner. That is why this measurement is so important.

Some possible solutions to shortening the delay contributed by the load are:

i. decrease the load capacitance.
ii. decrease the load resistance. It may be necessary to exceed the device load rating.

If load-contributed delay is still unmanageable, the tester can be programmed to calculate the load-contributed delay and subtract it from the measured value.

Section IV of this report goes into more detail regarding loading problems.

Miscellaneous Slash Sheet Changes

1. Pin capacitance measurements are done manually and are particularly time consuming since the values of capacitance are small and the number of measured pins per LSI package is large ($\approx$ 36). These measurements are normally performed only for initial qualification and after process or design changes which may affect the design capacitance.

A change was made to facilitate testing. A sample of five devices is fully tested for pin capacitance and then ten additional devices are chosen for further testing. The additional testing is focused upon the data and address outputs. These outputs are grouped according to design/construction similarities as described in "Data Logging" above.

One pin (the highest measured value found in the previous 5 test devices) is chosen from each group as representative of that group and measured for each of the 10 devices.

2. A change was made to allow the test programmer to make output logic level measurements at locations in the functional test convenient to the tester or test program. Previously these measurements were made at specified vectors.

3. The minimum-temperature test limits of subgroup 12 were deleted. Worst-case measurements for these devices occur at elevated temperature.

4. Table II Group B, C, and D test requirements were changed. For all three classes of devices, subgroup 12 was deleted and for subgroups 7 and 8, testing was limited for class B devices.

SECTION IV

LOADING FOR LSI DEVICES AND TRISTATE OUTPUTS

There are two basic loads favored by manufacturers and users to test T^2L type outputs. One load, shown in Figure 4-1a, is used for standard dynamic testing and the other, a variation of the first load, shown in Figure 4-4, is used for tristate propagation delay testing. With the emergence of complex LSI devices, automatic test equipment has become a necessity for comprehensive test capability for these devices. With the large number of outputs that most LSI devices have, the present loading methods precipitate problems such as limited space on tester load cards and tester provision for changing loads under program control. Discussed here are proposed loads and solutions to these problems.

Proposed T^2L Load

Testing of LSI devices has placed new requirements upon loading of integrated circuits. Because of device complexity and, in fact, the complexity of the applied test patterns, automatic testers such as the Fairchild Sentry and Tektronix 3260 are virtually a necessity. Testing LSI devices with large numbers of outputs has caused automatic tester cards to fill up rapidly with components when using the accepted T^2L load shown in Figure 4-1a. Another problem with LSI devices is that some are dynamic in nature. They must be continously cycled with test patterns in order to retain states necessary for making measurements such as VOL and VOH. Similar complex precondition patterns are necessary to place non-dynamic devices in their proper states although they do not require cycling of the pattern.

It would be advantageous to find one load that would use fewer components, have the characteristics of the accepted T^2L dynamic load, and be applicable to VOH, VOL testing. This would eliminate changing socket load cards and relays on socket cards for changing load configurations. It would provide a common load all manufacturers could use.

The proposed load (Figure 4-1b) is similar to the accepted T^2L load with the exception that it replaces the string of three diodes referenced to ground with a power supply voltage reference.

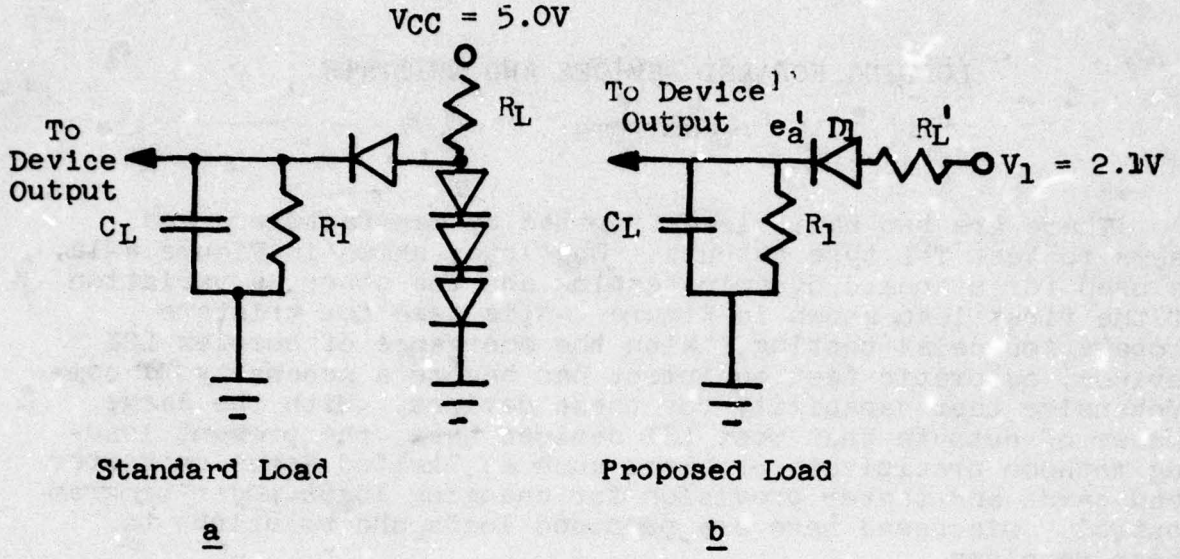


Figure 4-1. Load Circuits

Normally the value of R_L is chosen so that the device sink current is approximately 2/3 (IOL max). R_L' for the proposed load should be chosen so that the sink current is equal to maximum specified capability of the device under test. This allows VOH & VOL measurements to be made during dynamic measurements for complex devices.

The voltage V_1 of Figure 4-1b can be adjusted so that the voltage e_a' best suits the application. When making standard propagation delay measurements on devices that require a 1.5-volt reference point (Figure 4-2), V_1 should be chosen so that the load diode becomes forward biased at a voltage e_a' that is greater than the voltage reference point. In this case V_1 should equal approximately 2.5 volts. Where a reference voltage point of 1.3 volts is required, V_1 should equal approximately 2.1 volts. By avoiding a timing reference point that is at the voltage where the load diode switches, waveform discontinuities and changes in slope are also avoided.

For all tristate delay measurements V_1 ($\approx$ 2.1 V) is chosen so that e_a' (diode threshold) equals 1.5 volts (Figure 4-2). This places the end point voltage of the tristate level nearly equidistant between the standard worst-case T^2L logic levels.

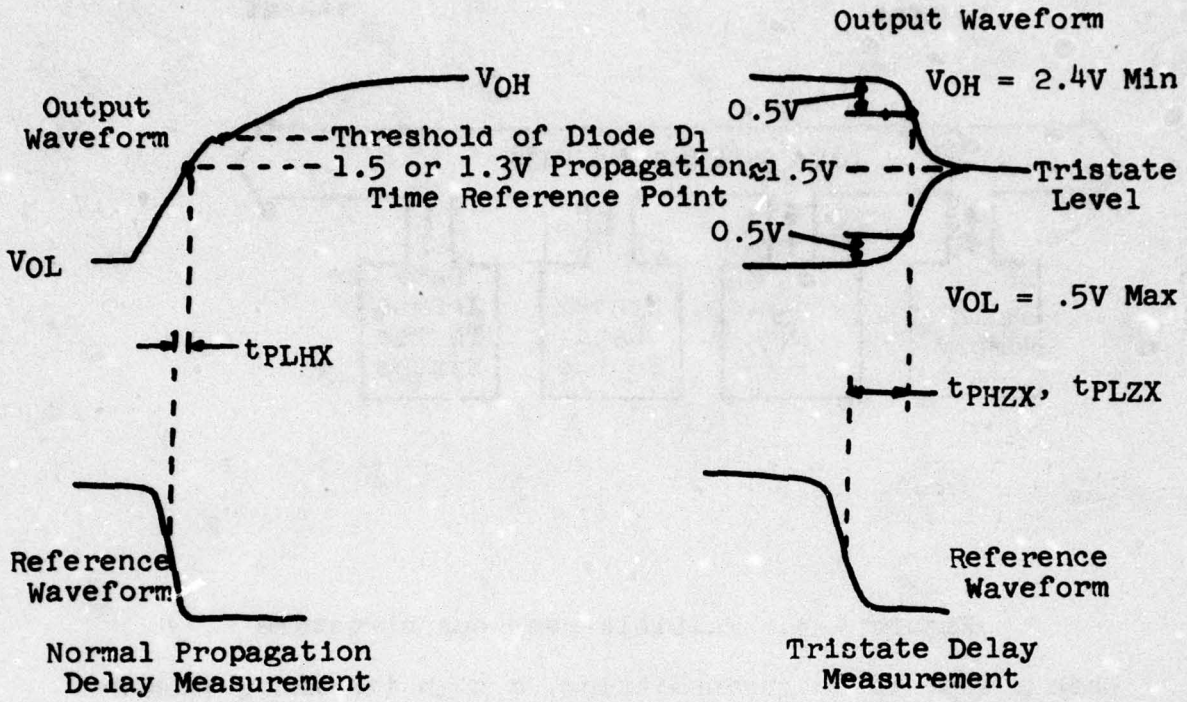


Figure 4-2. Propagation delay waveforms

Tristate Loading

Digital system designs are utilizing data-bus-oriented architecture. This is particularly true when considering microprocessors and their support chips. The theory is that multiple users of a data bus can transmit and receive on the bus provided that no two users transmit at the same time and that non-users present minimum loading to the bus. A possible multiple-user bus structure is shown in Figure 4-3.

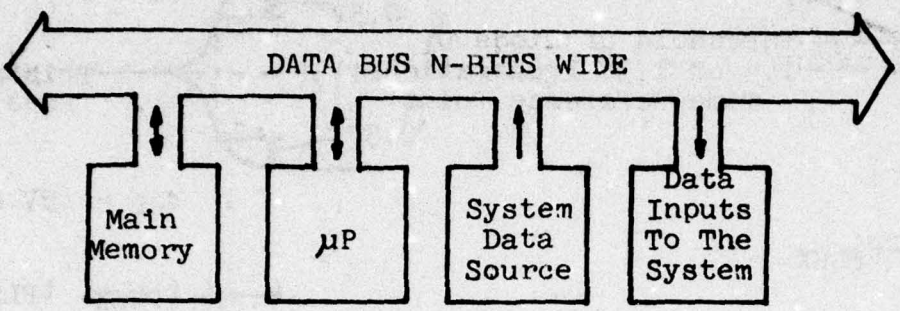


Figure 4-3. Multiple-user bus structure

When a user is not transmitting, a high impedance is presented to the bus (tristate). If the user can receive data also, the tristate load presented to the bus is generally in the several-hundred microamp range.

The purpose of the tristate propagation delay test is to determine how fast the high impedance state is reached compared to how quickly the device can switch from high impedance to a driven state. The goal is to quantify those times so that a designer will be able to determine the necessary tristate enable/disable system timing. The next bus user should be prevented from driving the bus before the previous user releases it. If two users momentarily try to drive the same bus to opposite logic levels, significant current transients can result. This will cause voltage spikes to occur on the bus with a good chance of the same occurring to device power supply lines. In practice, device tristate enable time is generally designed to be twice as fast as tristate disable time. Ideally the best way to check for this delay is without a capacitive load so that the measured delay will be predominantly throughput delay plus output transistor switching time delay. In a system configuration, after a device has released a bus, the bus capacitance will tend to maintain the voltage on it from the previous logic state. If system timing is such that the next user cannot wait for the bus to discharge, the next user must drive the bus to the desired state and sink the discharge current of the capacitance. Capacitive loading for dynamic tristate measurements, therefore, is not a requirement.

One of the most common tristate loads resembles the standard T^2L load with two switches added. The switch positions are a function of which of the four possible tristate level measurements is being made. If the tristate load requirements could be combined (with the other load requirements) into a single load, it would greatly simplify testing. A schematic of the most commonly used tristate load circuit is shown in Figure 4-4.

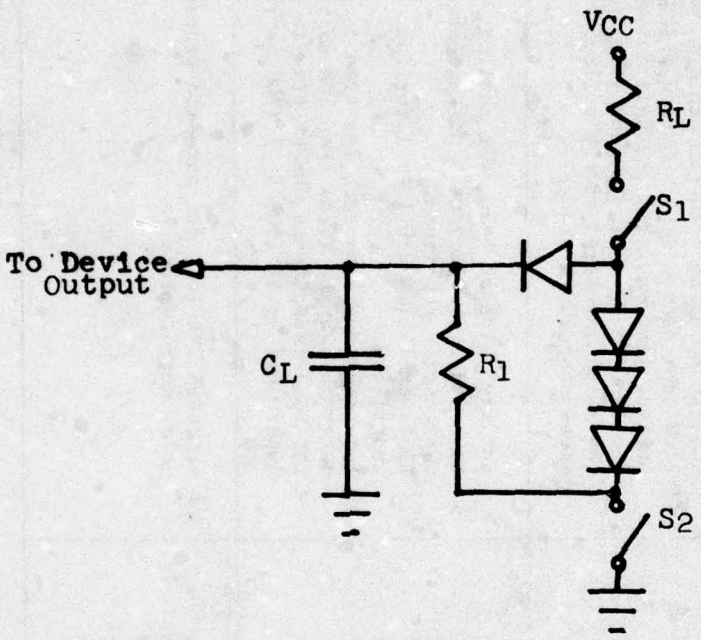


Figure 4-4. A commonly used tristate load

The load actually represents four separate loads when considering the various switch positions and different capacitive loading. Table 4-1 shows the various configurations.

Circuit configurations 1 and 2 of Table 4-1 have load-capacitance-charge-time constants similar to the proposed load of Figure 4-1. The major difference is that Table 4-1 loads have a full logic voltage swing. This does not appear to be necessary, nor is it a clear advantage.

Circuit configuration 3 of Table 4-1 is electrically the same as the proposed circuit. The major difference is that the capacitance loading was changed to reduce the long charge time constant incurred during the t_{PHZ} measurement. Five picofarads maximum loading is possible with a careful bench type test fixture, but it is not at all practical for automatic testers. Most automatic testers contribute 25 to 50 picofarads of loading through wiring and socket cards.

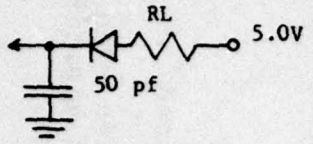
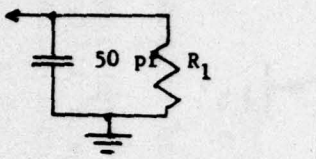
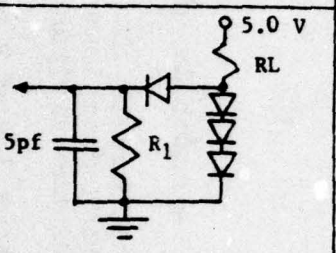
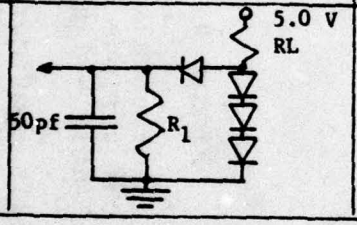
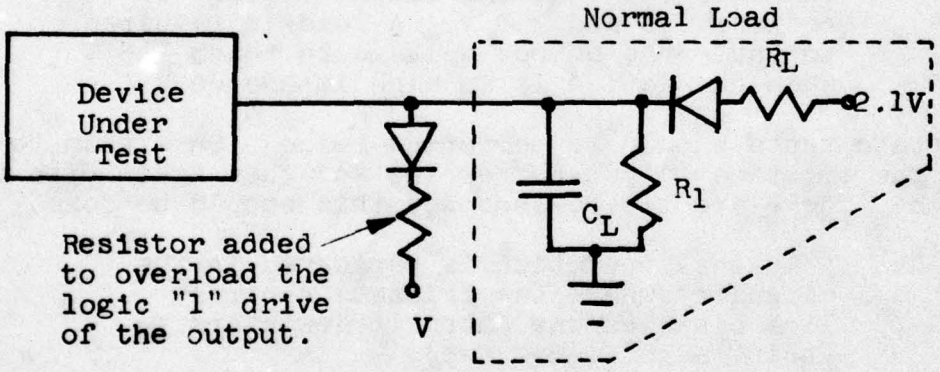
Ckt	Measurement	Switch Position	Circuit Configuration	Characteristics
1	t_{PZL}	S1 Closed S1 Open		i voltage swing at load (≈ 4.5 to VOL) ii load capacitance is discharged by the pull-down transistor dynamic on-impedance. Discharge time is determined by transistor characteristics (less than 100 ns range).
2	t_{PZH}	S1 Open S2 Closed		i voltage swing at load (VOH to VOL) ii load capacitance is discharged primarily by pull-up load resistor for full drive capability devices (≈ 50 - 150 Ω) and is a function of the switching speed of the pull-up transistor. (less than 100 ns range)
3	t_{PLZ} t_{PHZ}	S1 Closed S2 Closed		i voltage swing at load (VOL to 1.5V, VOH to 1.5 V) ii capacitance reduced to 5 pf to decrease load charge time constants. iii RL is small (≈ 250-1 K) for full T^2L drive capability. iv for t_{PLZ} capacitance charge time is primarily determined by RL (less than 100 ns). v for t_{PHZ} capacitance charge time is primarily determined by RL (≈6 K) (100 ns range).
4	t_{PLH} t_{PHL}	S1 Closed S2 Closed		i accepted T^2L load for standard propagation delay measurements.

Table 4-1. Various configurations and characteristics of Figure 4-4, tristate load

Tristate enable/disable device delay should not be swamped out by the charging of load capacitance. The problem generally occurs when a device does not have high current-drive capability; the logic "1" drive level of most all devices predominantly has the least drive. The resulting large values of load resistance present a problem with moderate capacitive loading (50 pf). Several possible solutions to this problem are outlined below:

1. Resistively overload the device for logic "1" current, (lower the effective value of R_1 Figure 4-1). Most devices are capable of a substantial amount of overdrive. This includes MOS devices but not to the level of T^2L.

   The logic "1" voltage level may be invalidated during this time. One method of achieving this, while still utilizing the recommended load of Figure 4-1, is shown in Figure 4-5. Essentially, the effective value of R_1 is lowered by switching in additional loading under tester program control.



NOTES: 1. The voltage (V) is under program control.
2. V = -.6 during tristate; +5.5 during normal testing.

Figure 4-5. Loading option for long RC charge time constants during tristate

2. Another alternative is to have the tester calculate the delay contributed by the load and subtract it from the measurement. This method can be very accurate, but it requires additional programming and data manipulation.

3. The load capacitance could be reduced to as low a value as practical.

Additional Testing Considerations for Tristate

There are two possible ways to verify if a device has gone into tristate during functional tests.

1. Force a voltage at the tristate output and measure a current. This must be done at 2.4 V or 5.5 V and again at 0.4 V. No load is required for this method.

2. Wait a specified time interval (for the output to reach its tristate level; $\approx$1.5 V) after enabling the tristate enable. Then check to see that the output voltage is between 1.0 and 2.0 V. A load is required to cause the output voltage to reach 1.5 V when the device is in high impedance.

Tristate tests should be performed twice. Once with the input to the tristate output buffer low and then again with the input high. There are two reasons why this should be done.

a. A logical operation is performed in the circuitry where the tristate control line disables the output transistors (point a in Figure 4-6).

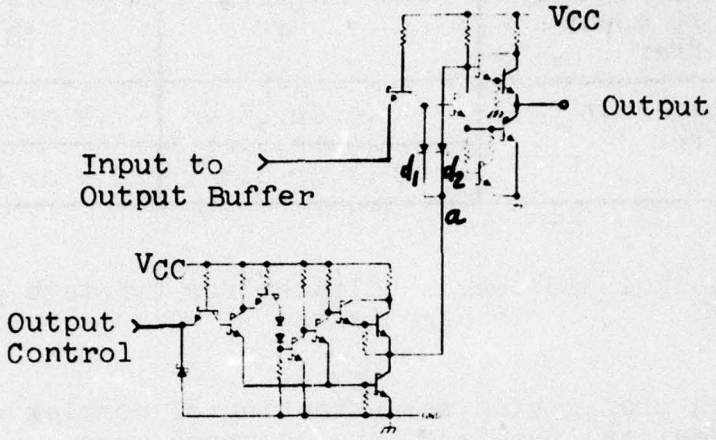


Figure 4-6. Test schematic

The tests should show that the diodes D1 and D2 each cause the pull-down and pull-up transistors to turn off respectively. This can only be accomplished if the output is disabled twice. Once when the input to the output buffers is a logic "1" and then again when it is a logic "0".

b. When measuring the three-state output leakage current during parameter testing, the output is usually forced to 2.4 or 5.5 volts and then to 0.4 or 0.5 volts (Table 4-2). Most methods used today require the three-state buffer element input line to be programmed to the opposite logic state of its output forcing voltage. Others do not specify preferred states. Practice has shown that these methods do not yield the worst-case current consistently. It is recommended that the leakage tests be repeated, for a logical "0" and "1", as input conditions to the output buffer.

Logic level at input to output buffer	"1"	"0"
Forcing voltages at tristate buffer outputs	.4 or .5 V	.4 or .5 V
	2.4 or 5.5 V	2.4 or 5.5 V

Table 4-2. Recommended test conditions for tristate output leakage tests

In propagation delay testing of complex devices, problems have occurred when going into the high-impedance mode. If the output buffers happen to be preloaded with a zero and the measurement is made from the logic "1" level to tristate, race conditions occur on the next device clock cycle. The device may try to go to logic "0" before it goes to tristate. The opposite is true if the measurement is from a logic "0" to tristate and the buffer is preloaded with a "1". In both cases an automatic tester could make the output delay measurement to the discontinuity that occurs at the output rather than to the "recovered" tristate waveform.

It is therefore recommended that tristate delay measurements for clocked complex devices be performed with specific preloaded logic levels on the output buffers. For a logic "1" to tristate delay measurement, the inputs to the tristate buffers should be preloaded with "1's". The inverse applies for a logic "0" to tristate level.

In summary, the proposed load of Figure 4-1 is recommended for T^2L type loading on future slash sheets. Where tristate propagation delay measurements constitute a problem because of large RC load time constants (limited drive capability of the device under test), there are several options:

a. Calculate the delay time attributable to the load and subtract it from the measurement.

b. Lower the effective load resistance during tristate. This would be accomplished under tester program control.

c. Reduce the load capacitance.

This load reduces component count, allows adjustment of the threshold of the loads' switching diode and provides a simple tri-state load for all users.

SECTION V

PROCEDURE FOR LSI FUNCTIONAL TEST DEVELOPMENT

This section describes the approach which was used for the evaluation of the functional tests for the 2901A.

This philosophy was developed and used on a previous microprocessor characterization effort for RADC, but was refined and formally documented for the first time on this contract.

The approach consists of the following steps.

1. Generate a detailed functional block diagram by partitioning the processor into basic functional blocks such as registers, multiplexers, arithmetic and logic functions and identifying all data paths.

2. Test each of the basic functional blocks using proven test patterns which result in a high Test Confidence Level (TCL). In some cases, these blocks can be exhaustively tested with few vectors.

3. Generate test patterns to verify the integrity of the data and control paths.

4. Verify that all instructions perform the specified operations.

5. Include test patterns that check for known processor sensitivities. This may include vendor and user-supplied data.

A gate-level diagram, timing diagram, and a block diagram which shows the major functional areas of the microprocessor and the interconnecting data and control paths would be valuable for test development/evaluation.

However, in many instances only a timing diagram and an insufficiently detailed block diagram are available. It is then necessary to develop a detailed functional block diagram based upon the best available information and verify its accuracy with the manufacturer.

Once this is done, verification that each of the functional blocks is tested using proven test patterns must be accomplished. Following is a list of the types of tests required.

1. Verify the independence of each IC pin. This is accomplished by checking that while each pin assumes a one and a zero state all of the other pins, either individually or collectively, are in the complement state. The states of input pins have to be monitored unless they are sensitized to the outputs.

2. Verify that the control lines perform the intended functions and perform independent of the previous instruction. This is accomplished by activating each control line and checking that address, data, and status lines assume the correct state. Independence is verified by activating the control lines in a gallop type test and checking the response.

3. Check that the proper priority is maintained when two or more control signals are applied at the same time.

4. Verify the high impedance capability of the applicable data and status lines by placing them in the high impedance state and measuring the leakage current. This should be done with the input of the three-state buffer driven to both a one and a zero.

5. Verify the independence of each line in a data path and that each line can pass a one and a zero. This is accomplished by checking that while each line assumes a one and a zero state. the others, either individually or collectively, are in the complement state.

6. Verify that any identifiable multiplexer can pass both a one and a zero in each selection position.

7. For serial arithmetic adders/subtractors with unknown mechanizations apply all possible inputs (0 & 0, 0 & 1, 1 & 0, 1 & 1) to each input pair with the carry equal to zero and then with the carry equal to one. This should be done in both the add and subtract modes. The carry is either the external carry into the adder or the carry from the next least significant bit. If the subtractor is a one or two's complement subtractor, these tests will also verify that the complementing circuitry can complement both a one and a zero.

8. For logic operations apply the following input conditions to each input pair of the ALU:

   0 & 0, 0 & 1, 1 & 0, 1 & 1 during EXOR operations

   0 & 0, 0 & 1, 1 & 0 during OR operations

   0 & 1, 1 & 0, 1 & 1 during AND operations

9. For shift left and shift right operations, verify the shift of 0 to 0, 0 to 1, 1 to 0, and 1 to 1 in each direction.

10. Check all flip-flops for 0 to 0, 0 to 1, 1 to 0, and 1 to 1 transitions.

11. Verify that the carry-in has no effect on the ALU during logic functions.

12. Verify that special outputs such as carry, carry generate, carry propagate, overflow, etc. from an ALU operate properly; i.e., assume both a one and a zero state and that they occur at the proper time. If equations are provided for their generation verify that each of the terms in the equations affects the outputs.

13. Verify the instruction set by performing each instruction or op code at least once. Checking that only the intended instruction is performed verifies that the decode circuitry is functioning properly.

14. Verify register independence, bit independence, and integrity of unique registers such as accumulators, stack pointers, index counters, storage registers, etc. Register independence is verified by writing into one of the registers and checking that the others are not affected. Bit independence is shown by having each bit in the zero and one state with respect to all other bits which are in the complement state. Integrity is verified by insuring that transitions from 0 to 0, 0 to 1, 1 to 0, and 1 to 1 are possible for each bit of each static register.

15. If the device contains a RAM, or the unique registers are configured as a RAM, the following items should be checked as a minimum.

a. Address Uniqueness - Verify that there are "W" independent word locations in a "W" word memory or that the unique registers are independent. This can be accomplished by writing into an address or register and verifying that it was the only address or register affected. The standard RAM tests which can be used for this are Walking-one, Walking-zero; Galloping-one, Galloping-zero; or Write Recovery.

b. Bit Independence - Show the independence of each bit in the zero and one state with respect to all other bits which are in the complement state. This can best be accomplished with the standard Walking-one, Walking-zero test.

c. Cell Integrity - Verify that transitions from 0 to 0, 0 to 1, 1 to 0, and 1 to 1 are possible for all bits. This can be accomplished with the Walking-one, Walking-zero test on RAM's that are more than one bit per word. For single-bit RAM's, separate tests have to be performed for the 0 to 0 and 1 to 1 transitions.

d. Intercell Disturbance (Dynamic RAM's only) - Maximize the number of internal transitions to test for cell-to-cell interaction. This can be accomplished with the standard Galloping-one, Galloping-zero test.

e. Data Retention (Dynamic RAM's only) - The test for data retention is described in Item 16.

15. (Continued)

It may be necessary to check the following items for certain devices.

a. Write Recovery - Verify that transitions from a write to a read do not cause access time failures. This is accomplished by checking all possible transitions from a write to a read.

b. Read Modify Write Recovery (Dynamic RAM's) - Verify that transitions from a read to a write do not cause incorrect information to be written into the device. This is accomplished by checking all possible transitions from a read to a write.

c. Sense Amplifier Recovery (Dynamic RAM's) - Test to insure that sense amplifiers respond properly to a complement bit after repeated reads of like data.

d. Sense Amplifier Response (Dynamic RAM's) - Test for sense amplifier frequency response by repeatedly reading 1-0 data patterns at minimum read cycle time.

16. Check dynamic registers and buses for proper operation. The test should verify that sufficient charge is transferred in the minimum transfer time and that sufficient charge is available after the maximum storage time. This is accomplished by varying the power supply voltages, and clock amplitudes, periods, widths, and delays to set up the worst case conditions described above.

SECTION VI

TEST DEVELOPMENT FOR THE 2901A MICROPROCESSOR

Introduction

This evaluation reviewed the proposed tests which Vendor A submitted for use in the slash sheet for the 2901A. The approach used to analyze these tests is presented in Section V. The logic block diagram which was used is from Vendor A's catalog and is shown in Figure 6-1.

Summary of Functional Test Evaluation

Two sets of Vendor A's functional tests were reviewed. The first set submitted for review was in place at Vendor A's facility and contained approximately 300 vectors. The analysis disclosed several deficient areas as follows:

1. All functions were not performed by the ALU.
2. All destination codes were not checked.
3. There were vectors where the expected results could be caused by more than one set of inputs -i.e., the expected output when performing D + Q could also be obtained by performing D + A.
4. It was not shown that C_n was irrelevant during logic functions.
5. Errors existed in the vectors -i.e., during shift tests the Y outputs were changing in reversed order of significance.

Prior to implementation of corrective action, a second set of functional tests was submitted for review. This set was more extensive and reflected Vendor A's improved test capability in a new automatic tester. This test vector set consisted of approximately 5000 vectors and was more consistent with modern test techniques for LSI devices.

After the initial evaluation of this set, Vendor A was contacted and the deficient areas were discussed. Vendor A agreed to incorporate many changes which would enhance the test. Since a modified version of the functional test had not been received from Vendor A at the time of the writing of this report it was decided to include the vectors which General Electric recommended for addition to the existing functional test.

Discussion

The following is a description of the evaluation.

1. When checking for pin independence it was found that approximate-

ly 93% of the 1256 combinations were included in the test. Vendor A was not receptive to changes in the test to improve this percentage. They indicated that if a short existed, it would be detected during parametric tests if it was not caught in the functional test. GE feels that the functional test should be a stand-alone test capable of detecting this type of fault. This allows the user to run only the functional test for screening purposes while maintaining a high level of confidence in the part. Therefore GE has included vectors to verify the independence of the remaining pin combinations.

2. The inputs that were considered as control lines were $\overline{0E}$ and I_{8-6}. $\overline{0E}$ was held low throughout the functional test thus keeping the Y outputs enabled. However, it should be taken high at points during the functional test where the high impedance capability of the Y outputs can be checked with the inputs of the buffers being driven both high and low. Vectors which accomplish this were added by GE.

   Control inputs I_{8-6} were exercised during the functional test. However, the $RAM_{3,0}$ and $Q_{3,0}$ outputs were don't cares in all but the RAM shift and Q shift tests. It was never verified that these three-state outputs which are connected to TTL inputs internal to the 2901A can ever go into the high impedance state. GE added vectors during which the destination codes are cycled through and these outputs are monitored.

3. The data paths in the 2901A were checked for independence. It was found that the four lines from the A latch to the Y outputs were always either all 1's or all 0's. When contacted, Vendor A replied that they were considering adding tests to cover this area. However, they added, some of the other existing tests would be affected if these lines were shorted since the inputs to the ALU would also be shorted. Further investigation by GE revealed the existence of a fault which could affect the Y outputs, but not the ALU inputs, and which would not be detected if the four lines were always all 0's or all 1's. GE added vectors that test for the above mentioned fault and show data path independence.

4. During verification of the multiplexers, a problem was found in the multiplexer on the S inputs of the ALU. The B inputs were never 1's when the multiplexer was supposed to pass a 0 through the Q or A inputs. This condition is required to show that the B select input is operating properly. Vectors were added to ensure proper operation of the multiplexer.

5. The parallel adder in the ALU was thoroughly tested in that all possible combinations of inputs were added to each other with the carry equal to zero and then with the carry equal to one. This test also verified the generation of $\overline{P}$, $\overline{G}$, C_{n+4}, and OVR by the ALU. Although all possible combinations were not performed during S-R and R-S subtraction they were not necessary. The only tests required here are for the inverters used ahead of the adder during subtraction. These were done.

   All four input combinations were applied to each set of inputs in the ALU during logic functions. However, it was not shown that C_n had no effect on the ALU during the logic functions. At first, Vendor A felt that because of the implementation of the carry in circuitry, it was not necessary to have $C_n = 1$. After further investigation they indicated that the test should be changed to verify the irrelevance of C_n during logic functions. GE added vectors which accomplish this.

6. The 2901A has nine instruction control lines which are used in groups of three to determine the source of the data to be operated on, the function performed by the ALU, and the destination of the result. The source, function, and destination codes are decoded by circuitry divided into three separate parts. This allows each group of three lines to be checked separately. The source and function codes were each cycled through their eight possible codes. However, the outputs of the source code tests are not unique -i.e. operating on A and B gives the same result as operating on 0 and A or D and Q. Vendor A agreed that the outputs of these tests should be unique. GE revised the source code tests to provide unique outputs and included these in the slash sheets.

   The function codes were checked thoroughly. The memory was preloaded with the content equal to the address. Then all of the functions were performed while operating on A and B. This was done for every set of A and B addresses and then with the A address equal to the inverse of the B address. This applied all four possible input combinations to each set of inputs on the ALU for both the arithmetic and logic functions.

   All of the destination codes were used during the test. However, the results were not always checked to verify that each one did what it was supposed to do.

The following problem areas existed in the check of the destination codes.

a. It was not verified that the RAM was not being loaded when octal code 0 was used.

b. It was not verified that the output of the ALU was being loaded into the RAM and that the Q register was not being loaded when octal code 2 was used.

Vendor A agreed that these codes should be checked and indicated that a modified RAM shift test and a modified Q shift test would test them. The added vectors which cycle through the destination codes thoroughly check all of them.

7. The vectors verified that the Q register and the RAM were independent. They also verified bit independence, cell integrity, and shift-left-shift-right operation of the Q register.

However, the Q register was never checked when the clock was low to verify that it was not written into on the high to low transition of the clock. GE feels that this should be checked to verify the proper operation of the Q register and has included this condition in the added vectors.

8. Address uniqueness, and shift-left-shift-right operation of the RAM were verified. The shift tests were performed only on address zero, but this was adequate since the multiplexers used for the shift operation are common to all addresses.

Cell integrity was partially checked. Additional vectors were added to the slash sheet by GE to complete these tests.

Bit independence was verified thoroughly for RAM address zero during the RAM shift test but only partially for the other addresses. Vendor A said that they would modify the RAM shift test to show bit independence for all addresses. GE repeated the existing RAM shift test for the other fifteen addresses.

Data from the RAM can be read through the A and B ports which are controlled by the A and B address lines respectively. It was verified that data could be read out through both ports at the same time and that they could be addressing the same or different memory locations. It was also verified that the A and B latches

are locked out when the clock is low and that they track the output of the RAM when the clock is high.

It was shown that the B address lines control the destination of data written into the RAM.

In test set 1 the RAM was loaded by cycling through the addresses and changing the data inputs while holding the clock low. Also the destination code was set up to load the RAM and the inputs to it changed while the clock was high. These two items verified that the RAM can be written into when the clock is low and is not changed when the clock is high. This was not included in the second set of vectors. GE feels it is important to verify the proper operation of the clock and has included these conditions in the added vectors.

9. The functional test for the 2901A was run at approximately 1 MHz. GE believes that running at the maximum clock rate provides a better test in that internal timing of the device would be worst-case checked. For the switching speed tests, the manufacturer selected the worst-case paths and these were the only ones exercised. Running the present functional test at speed (approximately 9 MHz) is not possible because many of the outputs may not stabilize in time. For example, a read-modify-write may be done on the RAM, but the new information has to propagate through the ALU to the outputs. This could take longer than the 110 nanosecond minimum clock period.

   As a compromise, the test should be run with a 200 nanosecond clock period. This is to allow for the worst-case set-up and propagation delay times of the device.

   A figure (13) was added to the slash sheet to cover the timing requirements for the functional test. The notes for the functional test were also clarified and the input levels changed to thresholds. Copies of the timing diagram and revised notes are included in Appendix A.

   GE also included a read-modify-write test and its timing diagram shown in Appendix A. This test is designed to run with a 110-nanosecond clock period.

Description of Added Vectors

The added vectors are divided into five sets which can be found in

Appendix A. The following describes the function of each set and where it should be inserted in Table V.

Set 1 - This set of vectors should be added to Test Group 33 between Test Numbers 0442 and 0443. It cycles through the eight function codes with $C_n = 1$ to verify that C_n is irrelevant during logic functions.

Set 2 - This set of vectors should replace Test Group 33, Test Numbers 0000 through 0022. It provides a source code test that has unique outputs.

Set 3 - This set of vectors should be added to Test Group 33 after Test Number 2735. It is the expanded RAM Shifting test which is used to verify bit independence for RAM addresses one through fifteen.

Set 4 - This set of vectors should be added as Test Group 44. It is the read-modify-write test for the RAM.

Set 5 - This set of vectors should be added as Test Group 30. It was added to accomplish the following:

1. Check the destination codes to verify that the RAM and Q register are properly loaded or left unchanged by each one. It also verifies that the RAM_3, RAM_0, Q_3, and Q_0 pins are in the high impedance state when they should be.

2. Show the independence of the data path from the A latch to the Y outputs.

3. Apply 1's to the B inputs of the S multiplexer while B is not selected to verify that the B select input is not S-A-1.

4. Apply many of the conditions required for the pin independence checks. The remainder were applied in the other added vectors.

5. Verify that the Y outputs are in the high impedance state when $\overline{OE} = 1$.

6. Check the Q register when the clock is low.

7. Load different RAM addresses by changing the B and D inputs while the clock is low.

8. Verify that data is not written into the RAM when the clock is high.

Summary of the Switching Speed Tests

This evaluation reviewed the switching speed tests which Vendor A had proposed for use in the slash sheet for the 2901A. The approach was different in that it proposed the use of algorithms to generate the input patterns.

To evaluate the tests, it was necessary to verify that the algorithms provided the patterns to measure all of the required switching parameters and that the worst-case paths were being exercised during the tests.

The initial review of the switching test information in the slash sheet for the 2901A revealed that it was deficient in many areas, and many questions were raised. The information presented was incomplete and confusing and, therefore, extremely difficult to evaluate. It was found that many changes would have to be made to complete and clarify the information provided.

Discussion

The following is a list of comments on the switching tests and GE's recommendations:

1. Table III C did not use standard symbols for the parameters being measured and it was not in the format used in other slash sheets. The format was revised and additional information, described in detail in the remaining comments, was added. A copy of the revised table (which is now labelled III B) is included in Appendix A.

2. The values in Table III C for the measured parameters did not agree with those given in the manufacturers' "Final Data" sheet dated June, 1977. Of greater importance, however, is the requirement that the values given can be met by all manufacturers of the 2901A. The values included in Table III B by GE are, in most instances, the worst-case value from the Vendor A and Vendor B data sheets and are given for -55°C and +125°C. The worst-case values (Vendor A) were not used for the propagation delays from any of the inputs to F_3 and $F = 0$. Their data sheet specifies the delay from any input to either the Y outputs or F_3 as being equal. This would indicate a zero delay through the multiplexer and tri-state buffers on the Y outputs. Also their delay from any input to $F = 0$ is 15 to 20 nanoseconds longer than the delay from the same input to the Y outputs. Vendor B specifies these delays as being approximately equal which is more reasonable based on the functional block diagram of the device.

Values for +25°C have to be obtained from the vendors since they should be tighter than those specified for the temperature extremes.

3. The timing diagram in the preliminary slash sheet was divided into three diagrams which were not sufficient in that they reflected the way Vendor A chose to do the test on their particular tester. GE expanded these into six diagrams (Figures 7 through 12 in the slash sheet) which are clearer and which show the parameters being measured. Copies are included in Appendix A.

4. Several of the patterns were identical and therefore unnecessary in the slash sheet. Patterns 1, 3, 6 and 8 were identical, 2 and 7 were identical, 4 and 9 were identical and 5 and 10 were identical. Vendor A said they were identified separately because each one is stored on a separate page in their tester memory. GE felt that only one pattern from each group should be included in the slash sheet. A vendor could duplicate and rename any pattern desired, if it makes programming or testing easier. Therefore, patterns 3, 6, 7, 8, 9, and 10 were eliminated and the others were renumbered as follows:

Old Number	New Number
1	1
2	2
4	3
5	4
11	5

Patterns 6, 7, and 8 which will be described later were also added.

The format of the old patterns was also tester oriented and at times difficult to follow. GE rewrote them in a more general language and also developed flowcharts for them. Copies of the revised patterns and the flowcharts are included in Appendix A.

5. The outputs of these patterns were not given so it was not apparent when a measurement should be made. Vendor A has their tester learn the outputs of the patterns by running a known good device and storing the results for future comparison. This is an acceptable method if the tester being used has the learn capability and if the known good device is, in fact, good. GE feels that a listing of the outputs should be included as part of the slash sheet and be available from DESC on request. This would make it possible for anyone to use the patterns without wading through them to determine when to make a measurement. GE requested and received listings of these

outputs from Vendor A. Reviewing them helped clarify the algorithms and also uncovered some errors in the algorithm listings in the slash sheet.

6. During the analysis of the patterns, it was found that some of them contained redundancies; i.e., the same group of lines were repeated or the same variable could be measured using different portions of the same pattern. Vendor A said some of the redundancies developed as the patterns were modified to allow measurements not previously done. Since deleting some of these might destroy the intent of the test it was decided not to change the patterns.

7. During the analysis of the patterns, the question arose whether or not the worst-case paths were being used for all of the measurements. For example, in all patterns except 4 and 5 the ALU is in the ADD mode. When asked about this, Vendor A replied that the worst-case path is being exercised in all cases. GE suggested running the switching tests at the same time as the functional tests thus guaranteeing that all possible paths are exercised. Vendor A said they set up separate tests because it is important to them to differentiate between functional and parametric failures. Without having access to a complete logic diagram for the 2901A, GE cannot verify that the worst-case paths are indeed being used. GE, however, did analyze each pattern to verify that, at a minimum, all paths between blocks were exercised.

   The paths from the A latch to the multiplexer on the R inputs of the ALU were never checked. This can be easily accomplished by running pattern 2 with the A inputs under test. This was added to Table III B for tests on the A inputs.

   Also not checked were the F→B and F→Q paths during the measurement of delays from the clock in pattern 4. Although the data sheet specifies that the clock is not in the critical speed path if the Q register is not a source, Vendor A could not provide an explanation of why the RAM and the A or B latch did not require as long a time to operate as the Q register. Therefore GE felt that the paths through the RAM should also be exercised. Tests were added to the end of pattern 4 to exercise the F→B and F→Q paths.

8. GE also found that certain set-up times and none of the hold times given on the data sheet were being measured in the slash sheet. The set-up times not measured are B destination, D (I = X 37), and RAM_0, RAM_3, Q_0, Q_3. Also, the switching tests are done with the clock input at its minimum low width but never at its minimum high width, minimum

period, or maximum frequency to shift the Q register. When questioned about this, Vendor A said that these tests were done on the bench. Whether they are done on an automatic tester or on the bench they should be incorporated into the slash sheet.

In addition, the set-up times for C_n and the D inputs were not measured while they could affect loading of the Q register. The set-up time for C_n was measured only when it was affecting address zero of the RAM.

Patterns 1 and 3 have been modified to allow these measurements to be made on C_n and the D inputs. Pattern 6 was added to measure the set-up times for B destination and D (I = X37). Measurement of most of the hold times was incorporated into the combinational propagation delay time tests by having the return to complement occur after a hold time of 0 nanoseconds. Patterns 7 and 8 were added to measure the set-up and hold times for Q_3, Q_0, RAM_3 and RAM_0.

The minimum high time and maximum frequency to shift the Q register were incorporated into the functional test which is now going to be at 5 MHz. GE added a read-modify-write test which is run at the minimum-clock period.

9. It was also found that Table I did not specify any of the parameters that were being measured in the switching tests. These were added and a copy of the revised Table is included in Appendix A. The loads called out for the switching tests have also been modified to better represent what the device will see in actual use. The device is now run at full load during the switching tests. Also, the revised load can be used on three-state outputs without requiring the opening and closing of switches as was necessary with the previous load. A copy of the new loads is included in Appendix A.

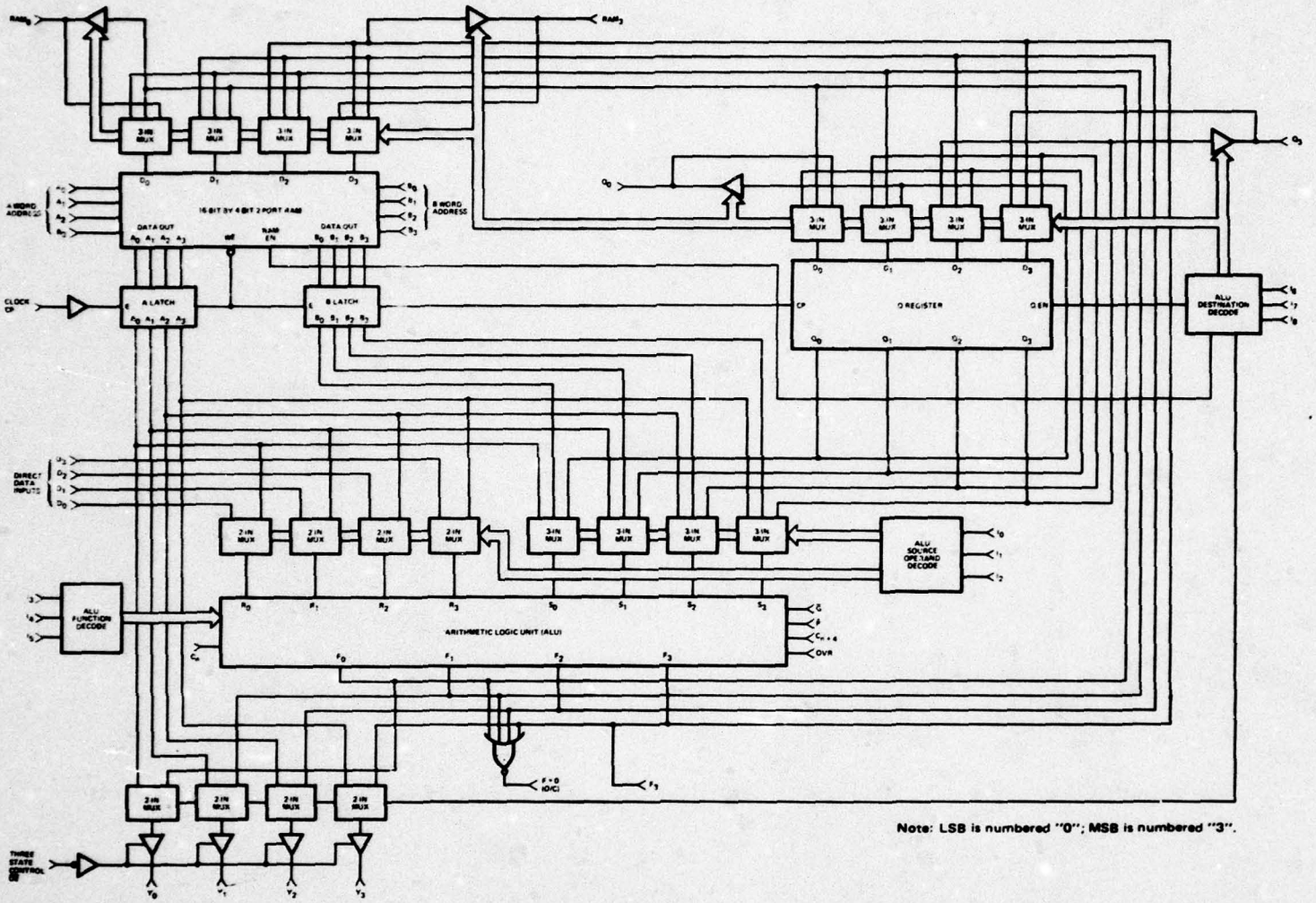


FIGURE 6-1. 2901A BLOCK DIAGRAM

SECTION VII

GENERATION OF LOGIC INTEGRITY TESTS FOR THE 8212

Introduction

Test vector development for the 8212 consisted of the following:

1. hand generation of an initial vector set
2. computer simulation to check the test vector effectiveness for Vendor C's 8212
3. modification of the vector set to catch undetected faults
4. computer simulation to check the test vector effectiveness for Vendor D's 8212
5. modification of the set to check undetected faults
6. development of Tektronix S-3260 test
7. testing of devices with test vectors

Circuit Description

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor. The device can be used to implement latches, gated buffers or multiplexers.

Vector and Model Development

Figures 7-1 and 7-2, respectively, illustrate Vendor C's and Vendor D's 8212 implementation. The devices are functionally identical, but have differences in their combinational circuits.

The D-LASAR computer simulation required that both 8212's be modeled at the gate level. Since the exact implementation of the service request (SR) and the data flip-flops is unknown, models were chosen based upon the manufacturer's functional descriptions.

The SR flip-flop was modeled as the D-type flip-flop shown in Figure 7-3. This model was suggested by the D-LASAR user's manual as one that would not exhibit race conditions that the simulation program could not handle.

The data latch model is shown in Figure 7-4. It has the following characteristics:

1. Input data is latched to the output when the clock goes from 1 to 0.

2. The reset input is effective only when the clock is at 0.

3. When the clock is 1 (reset can be 1 or 0), the output tracks the input.

Since the eight data latches are identical, only one was included in the computer simulation model. This simplification saved computing time since the program would have treated each latch separately and generated an unncessarily large number of vectors.

Results of Vendor C's 8212 Simulation

The program evaluated the 34 hand-generated vectors on Vendor C's 8212, added three buffer vectors to prevent race-conditions, and listed several failures that were not caught. These 37 vectors (1 - 37 in Table 7-1) result in a Test Confidence Level (TCL) of 92.6%. Three of the failures not caught are undetectable. These are stuck-at-one (S-A-1) failures indicated by the Xs in Figure 7-3. The remaining failures not caught were a stuck-at-zero (S-A-0) fault on an input of the NOR gate feeding the SR flip-flop (Figure 7-1) and faults that can be detected by placing the output drivers in the high impedance (HiZ) state and checking output leakage.

Since the gate level implementation of the latches is unknown, all possible input conditions were applied to the latches by appending the vector set.

Figure 7-5 lists all possible conditions for the SR flip-flop. A ↑ indicates a 0 to 1 transition, a ↓ indicates the inverse. Figure 7-6 lists all possible input conditions for the data latches. Next to each input in Figure 7-5 and 7-6 are two numbers corresponding to the vectors, from Table 7-1, that provide the input conditions. Since vectors 1 through 37 cover the majority of latch input conditions, it was certain that the remaining input conditions could be checked without a large expansion of the vector set. Thus, vectors 38 through 56 in Table 7-1, were added to cover the input conditions and to cover the S-A-0 fault at the NOR gate input. Finally, 8 more vectors (57 - 64) were added to verify the independence of each data latch. (Three input conditions to the SR flip-flop were inadvertently left unchecked by the vector set developed thus far. The unchecked conditions were later covered by vectors 70 - 73).

Vendor D 8212 Simulation

Examination of Vendor D's implementation revealed that although the combinational network performed a function identical to the network in Vendor C's device, the required test vectors were not necessarily identical. The latches might not be implemented identically to Vendor C's, but they are tested exhaustively by vectors 1 through 56, and therefore need no additional consideration.

Vendor D's device (with only one data latch) was simulated using the D-LASAR program. Vectors 1 through 56 were applied. The results indicated that a stuck-at-one fault was not checked on the gate input marked by an X in Figure 7-2. Thus, vectors 65 through 69 were added to insure a check on this fault.

The last group of vectors in Table 7-1 placed the drivers in the HiZ state. By performing output leakage tests the HiZ state is verified.

All the vectors in Table 7-1 constitute a 100% TCL for functional testing (assuming the leakage tests are performed) of Vendor C's and D's 8212s.

3260 Test

A test program was developed to be run on the Tektronix 3260 tester. This program functionally tests the device by applying the set of input vectors described above to the device and checking the resulting output states against the expected output vectors. Included in the program are several propagation delay measurements. The reference Table for these measurements is Table 7-2. Appendix B contains the wiring list for the socket card, a copy of the test program, test pattern file, pin assignment program, and load card diagram.

Table 7-1. Test vectors

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																									MEASUREMENT TERMINAL
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24		
			TEST NO.	$\overline{DS_1}$	MD	DI_1	DO_1	DI_2	DO_2	DI_3	DO_3	DI_4	DO_4	STB	GND	DS_2	$\overline{CLR}$	DO_5	DI_5	DO_6	DI_6	DO_7	DI_7	D08	DI8	$\overline{INT}$	V_{CC}		
7(T_A = 25°C)	Truth Table Test	3014	1	B	A	B	L	B	L	B	L	B	L	B		B	B	L	B	L	B	L	B	L	B	H		All Outputs
			2		A											A	B									L		
			3		B											B	B									L		
			4		B											B	A									L		
			5		A	A		A		A		A				A			A		A		A		A	L		
			6				H		H		H		H					H		L		H					L		
			7				H		H		H		H					H		L		H					L		
			8				H		H		H		H					H		L		H					L		
			9				H		H		H		H					H		L		H					L		
			10				H		H		H		H					H		L		H					L		
			11				L		L		L		L				B	L		H		L					H		
			12		B		H		H		H		H					H		H		L					L		
			13			B	H	B	H	B	H	B	H	A		A		H	A	H	B	H	A	H	B	H	L		
			14			A	H	A	H	A	H	A	H	A		A		H	A	H	A	H	A	H	A	H	L		
			15			A	H	A	H	A	H	A	H	A		A		H	A	H	A	H	A	H	A	H	L		
			16			A	H	A	H	A	H	A	H	A		A		H	A	H	A	H	A	H	A	H	L		
			17			A	H	A	H	A	H	A	H	A		A		H	A	H	A	H	A	H	A	H	L		
			18			A	H	A	H	A	H	A	H	A		A		H	A	H	A	H	A	H	A	H	L		
			19			A	H	A	H	A	H	A	H	A		A		H	A	H	A	H	A	H	A	H	L		
			20			A	H	A	H	A	H	A	H	A		A		H	A	H	A	H	A	H	A	H	L		
			21			A	H	A	H	A	H	A	H	A		A		H	A	H	A	H	A	H	A	H	L		
			22			A	H	A	H	A	H	A	H	A		A		H	A	H	A	H	A	H	A	H	L		
			23			A	H	A	H	A	H	A	H	A		A		H	A	H	A	H	A	H	A	H	L		
			24		A																								
			25	A		A	H	A	H	A	H	A	H	A		A		H	A	H	A	H	A	H	A	H	H		
			26														A												
			27			A	H	A	H	A	H	A	H	A		A	A	H	A	H	A	H	A	H	A	H	H		

GND

4.5

NOTES:
1. L = 0.45V Max H = 3.65V Min
2. A = 2.0V B = 0.85V
3. Z = High Impedance State
   I_{OZ} = ± 20 μA Max at V_O = .45 and 4.5V

Table 7-1. Test vectors - (Continued)

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE / TEST NO.	1 $\overline{DS_1}$	2 MD	3 DI_1	4 DO_1	5 DI_2	6 DO_2	7 DI_3	8 DO_3	9 DI_4	10 DO_4	11 STB	12 GND	13 DS_2	14 $\overline{CLR}$	15 DO_5	16 DI_5	17 DO6	18 DI6	19 DO7	20 DI_7	21 DO8	22 DI_8	23 $\overline{INT}$	24 VCC	MEASUREMENT TERMINAL
7 (T_A = 25°C)	Truth Table Test	3014	28	A	A	B	L	B	L	B	L	B	L	B	GND	A	A	L	B	L	B	L	B	L	B	L	4.5	All Outputs
			29			B	L	B	L	B	L	B	L	B		A	B		B		B		B		B	H		
			30			A	L	A	L	A	L	A	L	B		A	B		A		A		A		A	H		
			31	B			H		H		H		H	B		A	B	H		H		H		H		L		
			32											B		A	A									L		
			33											A		A										L		
			34											A		B										H		
			35											B												L		
			36											A												L		
			37				L		L		L		L	A			B	L		L		L		L		H		
			38											A			A									H		
			39											B												L		
			40											A												L		
			41											B												L		
			42				H		H		H		H			A		H		H		H		H		L		
			43				H		H				H			B		H		H		H		H		H		
			44				H		H				H			A		H		H		H		H		L		
			45			B	H	B	H	B		B	H					H	B	H	B	H	B	H	B			
			46				L		L		L		L				B	L		L		L		L				
			47														A											
			48		B												A											
			49														B											
			50			A		A		A		A					A		A		A		A		A			
			51			A		A		A		A					B		A		A		A		A			
			52			B		B		B		B					B		B		B		B		B			
			53		A	A	H	A	H	A	H	A	H				A	H	A	H	A	H	A	H	A			

NOTES:
1. L = 0.45V Max   H = 3.65V Min
2. A = 2.0V   B = 0.85V
3. Z = High Impedance State
$I_{OZ} = \pm 20\ \mu A$ Max at V_O = .45 and 4.5V

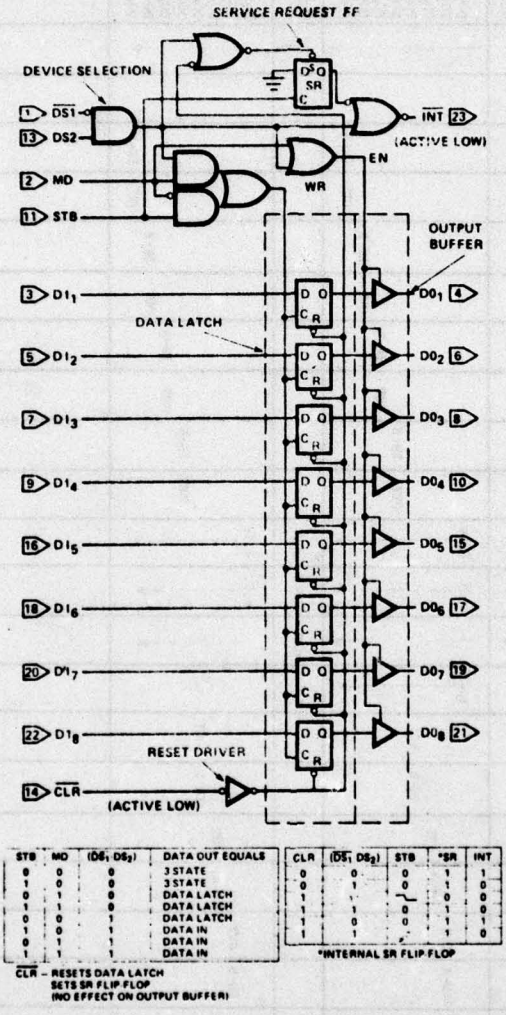
Table 7-1. Test vectors - (Continued)

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE / TEST NO.	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																								MEASUREMENT TERMINAL
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
				$\overline{DS_1}$	MD	DI_1	DO_1	DI_2	DO_2	DI_3	DO_3	DI_4	DO_4	STB	GND	$\overline{DS_2}$	$\overline{CLR}$	DO_5	DI_5	DO_6	DI_6	DO_7	DI_7	DO_8	DI_8	$\overline{INT}$	V_{CC}	
7 (T_A = 25°C)	Truth Table Test	3014	54	B	B	A	H	A	H	A	H	A	H	B	GND	A	A	H	A	H	A	H	A	H	A	L	4.5	All Outputs
			55		B	B		B	H	B	H	B	H					H	B	H	B	H	B	H	B			
			56		B	A		A	H	A	H	B	H					L	A	L	A	L	A	L	A			
			57		A	A		B	L	B	L	B	L					L	B	L	B	L	B	L	B			
			58			B	L	A	H	A	L	B	L					L	B	L	B	L	B	L	B			
			59			A		B	L	B	H	B	L					L	B	L	B	L	B	L	B			
			60			B		A	L	A	L	A	H					L	B	L	B	L	B	L	B			
			61			A		B	L	B	H	B	L					L	B	L	B	L	B	L	B			
			62			B		A	L	A	L	A	H					L	B	L	B	L	B	L	B			
			63			A		B	L	B	H	B	L					L	B	L	B	L	B	L	B			
			64			B		A	L	A	L	A	H					L	B	L	B	L	B	L	B			
			65			A		B	L	B	H	B	L					L	B	L	B	L	B	L	B			
			66			B		A	L	A	L	A	H	A				L	B	L	B	L	B	L	B			
			67		B	A	Z	A	Z	A	Z	A	Z	B		B	B	Z	A	Z	A	Z	A	Z	A	H		
			68		B	B	Z	B	Z	B	Z	B	Z	A		A	A	Z	B	Z	B	Z	B	Z	B			
			69		A	B	H	A	H	A	H	A	H	B		B	B	Z	A	Z	A	Z	A	Z	A			
			70		B	B	Z	B	Z	B	Z	B	Z	A		A	A	Z	B	Z	B	Z	B	Z	B			
			71		B	B	Z	B	Z	B	Z	B	Z	B		B	B	Z	A	Z	A	Z	A	Z	A			
			72		B	B	Z	B	Z	B	Z	B	Z	B		B	A	Z	B	Z	B	Z	B	Z	B			
			73		B	B	Z	B	Z	B	Z	B	Z	B		B	B	Z	A	Z	A	Z	A	Z	A			
8	Same tests, terminal conditions and limits as for subgroup 7, except T_A = 125°C and -55°C.																											

NOTES: 1. L = 0.45V MAx H = 3.65V Min
2. A = 2.0V B = 0.85V
3. Z = High Impedance State
I_{OZ} = ± 20 µA Max at V_O = .45 and 4.5V

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	MEASUREMENT TERMINAL	TEST LIMITS		
			TEST NO.	$\overline{DS_1}$	MD	DI_1	DO_1	DI_2	DO_2	DI_3	DO_3	DI_4	DO_4	STB	GND	DS_2	$\overline{CLR}$	DO_5	DI_5	DO_6	DI_6	DO_7	DI_7	DO_8	DI_8	$\overline{INT}$	V_{cc}		MIN	MAX	UNITS
9 T_A = 25°C	t_{PHL1}	3003	163 164 165 166 167 168 169 170	GND	4.5V	IN-A	OUT	IN-A	OUT	IN-A	OUT	IN-A	OUT		GND	4.5V	4.5V	OUT	IN-A	OUT	IN-A	OUT	IN-A	OUT	IN-A		5.0V	DO_1 DO_2 DO_3 DO_4 DO_5 DO_6 DO_7 DO_8		30	ns
	t_{PHL2}		171 172 173 174 175 176 177 178		GND	IN-B	OUT	IN-B	OUT	IN-B	OUT	IN-B	OUT	IN-C		GND	4.5V	OUT	IN-B	OUT	IN-B	OUT	IN-B	OUT	IN-B			DO_1 DO_2 DO_3 DO_4 DO_5 DO_6 DO_7 DO_8		37	ns
	t_{PHL3}		179	GND										IN-D	GND	IN-E	4.5V									OUT		$\overline{INT}$		37	ns
	t_{PHLA}		180 181 182 183 184 185 186 187	IN-C	4.5V	IN-B	OUT	IN-B	OUT	IN-B	OUT	IN-B	OUT			4.5V	4.5V	OUT	IN-B	OUT	IN-B	OUT	IN-B	OUT	IN-B			DO_1 DO_2 DO_3 DO_4 DO_5 DO_6 DO_7 DO_8		37	ns

Table 7-2. References for propagation delays



STB	MD	($\overline{DS_1}$, DS_2)	DATA OUT EQUALS
0	0	0	3 STATE
1	0	0	3 STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

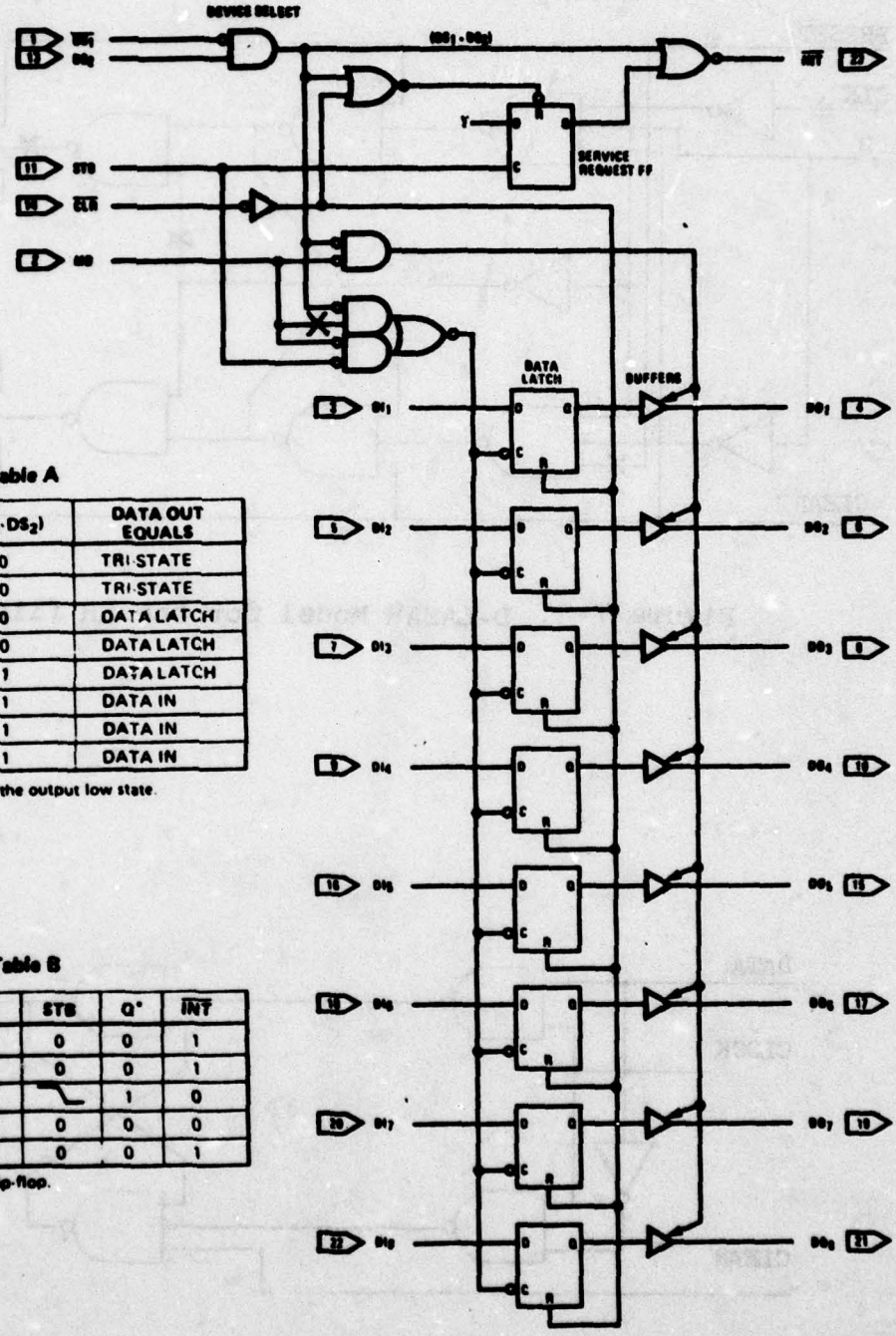
CLR – RESETS DATA LATCH
SETS SR FLIP FLOP
(NO EFFECT ON OUTPUT BUFFER)

CLR	($\overline{DS_1}$, DS_2)	STB	*SR	INT
0	0	0	1	1
0	1	0	1	0
1	1	↓	0	0
1	1	0	1	0
1	0	0	1	1
1	0	↓	1	0

*INTERNAL SR FLIP-FLOP

Figure 7-1. Vendor C's 8212 eight bit port

DP8212 logic diagram



Logic Table A

STB	MD	$(DS_1 \cdot DS_2)$	DATA OUT EQUALS
0	0	0	TRI-STATE
1	0	0	TRI-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

$\overline{CLR}$ ⌐ resets data latch to the output low state.

Logic Table B

$\overline{CLR}$	$(DS_1 \cdot DS_2)$	STB	Q*	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	⌐	1	0
1	1 RESET	0	0	0
1	0	0	0	1

*Internal Service Request flip-flop.

Figure 7-2. Vendor D's 8212

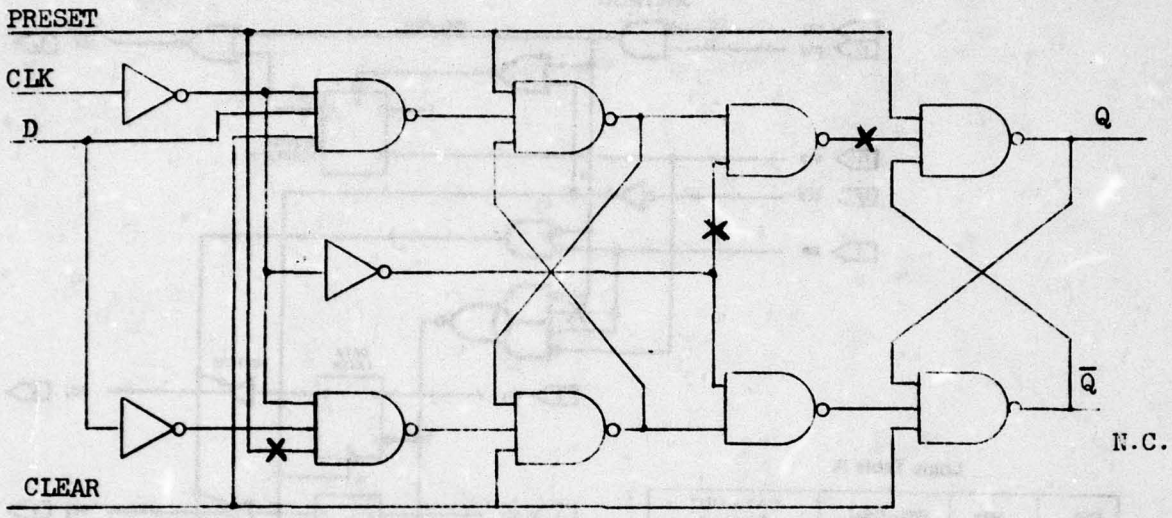


Figure 7-3. D-LASAR Model for the SR flip-flop

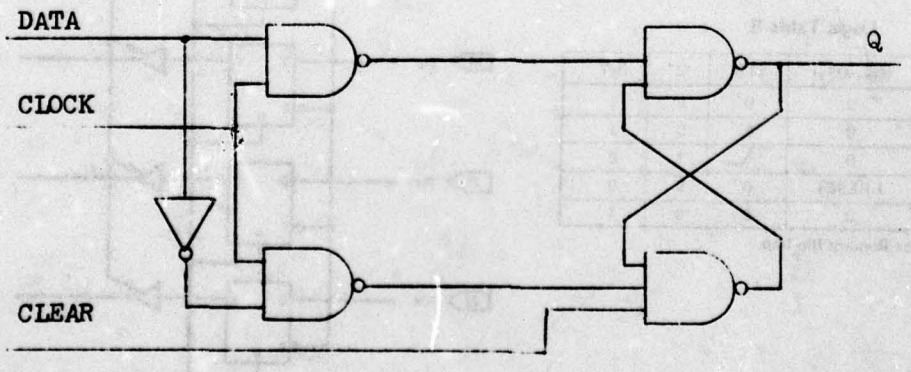


Figure 7-4. Clocked data latch

S	C	Before Vector Q	Covering Vector(s) from Figure 7
0	↑	1	32 - 33
0	↓	1	70 - 71
1	↑	0	35 - 36
1	↓	0	40 - 41
1	↑	1	26 - 27
1	↓	1	27 - 28
↓	0	0	28 - 29
↑	0	1	42 - 43
↓	0	1	72 - 73
↓	1	0	36 - 37
↑	1	1	33 - 34
↓	1	1	69 - 70

Figure 7-5. Possible inputs to SR flip-flop

D	$\overline{R}$	C	Before Vector Q	Covering Vector From Figure 7
0	0	↑	0	1-2
0	0	↓	0	2-3
0	1	↑	0	4-5
0	1	↓	0	5-6
0	1	↑	1	18-19
1	0	↑	0	12-13
1	0	↓	1	11-12
1	1	↑	0	7-8
1	1	↑	1	9-10
1	1	↓	1	8-9
0	↑	0	0	3-4
0	↓	0	0	48-49
0	↓	0	1	22-23
0	↑	1	0	46-47
0	↓	1	0	45-46
1	↑	0	0	37-38
1	↓	0	0	50-51
1	↓	0	1	36-37
1	↑	1	1	15-16
1	↓	1	1	10-11
↑	0	0	0	29-30
↓	0	0	0	51-52
↑	0	1	0	14-15
↓	0	1	1	13-14
↑	1	0	0	6-7
↓	1	0	0	27-28
↑	1	0	1	55-56
↓	1	0	1	17-18
↑	1	1	0	19-20
↓	1	1	1	44-45

Figure 7-6. Possible data latch inputs

SECTION VIII

DEVELOPMENT OF A LOGIC INTEGRITY TEST FOR THE 2918 QUAD D REGISTER

Objective

Develop Logic Integrity tests for the 2918 Quad D Register with standard and three-state outputs.

Circuit Description

The 2918 is a quadruple D-type register with four standard totem pole,outputs and four three-state bus-type outputs. It is a 16-pin device that also features a buffered common clock (CP) and a buffered common output control ($\overline{OE}$) for the Y outputs. The same data that is on the Q outputs is enabled at the three-state Y outputs when $\overline{OE}$ input is LOW. When $\overline{OE}$ input is HIGH, the Y outputs are in the high impedance state. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

Vector Generation

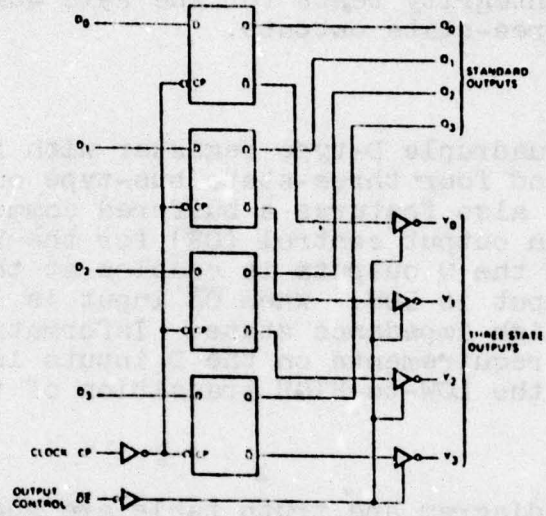
The 2918 logic diagram and truth table are shown in Figure 8-1. The 2918 test vectors were generated by hand. All possible input combinations, which are listed in Figure 8-2, are applied to each D-type flip-flop. The tests on the D0 and D2 latches are staggered relative to those on the D1 and D3 latches to verify isolation between the two pairs. The last eight vectors in Table 8-1 check the disabled state on the high impedance outputs and verify isolation between D0 and D2 and between D1 and D3.

The vector set produces a 100% Test Confidence Level (TCL). Since the set is exhaustive, the vectors will test any implementation of the 2918 as long as it is functionally identical to Vendor A's device.

3260 Test

A test program was developed for a Tektronix 3260 automatic tester. This program functionally tests the device by applying the set of input vectors described above to the device and checking the resulting output states against the expected output vectors. It also tests for leakage while the Y outputs are in the high impedance state. Appendix C contains the wiring list for the socket card, a copy of the test program, pin assignment program and test pattern file.

LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

Figure 8-1. 2918 logic diagram and truth table

INPUTS		OUTPUTS	
D	CP	Before Vector Q	Response Q
0	↑	0	0
0	↑	1	0
0	↓	0	0
0	↓	1	1
1	↑	0	1
1	↑	1	1
1	↓	0	0
1	↓	1	1
↑	0	0	0
↓	0	1	1
↑	1	0	0
↓	1	1	1

Figure 8-2. Exhaustive test set for 2918 latch

↑ Indicates a 0 to 1 transition

↓ Indicates a 1 to 0 transition

Table 8-1. Functional test vectors

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																MEASUREMENT TERMINAL
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
			TEST NO.	D_0	Q_0	Y_0	D_1	Q_1	Y_1	$\overline{OE}$	GND	CP	Y_2	Q_2	D_2	Y_3	Q_3	D_3	V_{CC}	
7 (T_A = 25°C)	Truth Table Test	3014	1	B	X	X	A	X	X	B	GND	A	X	X	B	X	X	A	4.5V	All Outputs
			2		X	X		X	X			B	X	X		X	X			
			3		L	L		H	H			A	L	L		H	H			
			4									B								
			5	A			B					A			A			B		
			6									B								
			7		H	H		L	L			A	H	H		L	L			
			8									B								
			9									A			A			B		
			10	B			A					A			B			A		
			11									B								
			12									A			A			B		
			13									B								
			14									A			A			B		
			15									B								
			16									A			A			B		
			17		L	L		H	H			A	L	L		H	H			
			18									B								
			19									A			A			B		
			20									B								
			21									A			A			B		
			22									B								
			23					L	L			A			A			B		
			24					L	L			B								
			25					H	H			A			A			B		
			26		H	H		H	H			B	H	H		L	L			
			27		H	H		H	H			A	H	H		H	H			
			28		H	H		Z	Z			B	Z	Z		Z	Z			
			29		Z	Z		L	L			A	H	H		H	H			
			30		L	L		H	H			B	Z	Z		Z	Z			
			31					L	L			A			A			B		

Table 8-1. (Cont'd)

Notes:

1. Tests must be run in sequence shown.
2. A = 2.0V; B = 0.8V
3. H = 2.4V Min on Y outputs, 2.5V Min on Q outputs; L = 0.5V Max
4. X = Don't Care
5. Z = High Impedance State, $I_{OZ} = \pm 50$ uA at V_O = 2.4V and 0.4V

SECTION IX

DEVELOPMENT OF LOGIC INTEGRITY TESTS FOR THE 2905, 2906, 2907, 2915, 2916, AND 2917 QUAD BUS TRANSCEIVERS

Objective

Develop Logic Integrity Tests for the 2905, 2906, 2907, 2915, 2916, and 2917 Quad Bus Transceivers (MIL-M-38510/441).

Circuit Description

The 2905, 2906, 2907, 2915, 2916 and 2917 are high-performance, low-power Schottky bus transceivers. The devices consist of four D-type edge-triggered flip-flops with a buffered common clock. This common clock (DRCP) enters data into the flip-flop registers on the low-to-high transition. The 2915, 2916 and 2917 flip-flop outputs are connected to four three-state bus drivers. The 2905, 2906 and 2907 flip-flop outputs are connected to four open-collector bus drivers. The data from the D-type flip-flop is inverted at the bus output. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches and are non-inverted from the driver input to D-type latch output. The four latches are controlled from the buffered receiver enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the latch outputs will follow the bus inputs. When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The 2905, 2907, 2915 and 2917 D-type latches have three-state inverter-buffer outputs. The output state is controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state. The 2906 and 2916 D-type latch outputs contain an inverter-buffer on their outputs.

The 2905, 2906, 2915 and 2916 inputs to the four D-type flip-flops contain a built-in two-input multiplexer. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The 2907 and 2917 contain a non-inverting buffer on the inputs to the D-type flip-flops.

The 2906, 2907, 2916 and 2917 feature a built-in odd parity checker/generator. The bus enable ($\overline{BE}$) input controls whether the parity output is in the generate or check mode.

When $\overline{BE}$ is LOW (driver enable), odd parity is generated based on the input to the D-type flip-flop. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and, if the driver is in the high-impedance state, the BUS parity is checked.

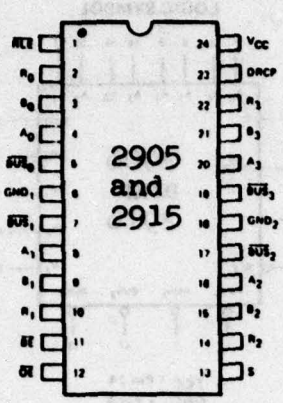
Vector Generation

The logic diagrams for the 2905 and 2915 (Fig. 9-1C), 2906 and 2916 (Fig. 9-2C), and 2907 and 2917 (Fig. 9-3C) were reviewed and the circuit mechanizations were found to be functionally correct. It was determined that although the three devices perform similar functions, developing common test vectors for all three devices was not practical because of circuitry differences i.e., multiplexers and parity generators. The test vectors were generated by hand. All possible input combinations are applied to the flip-flops and all "stuck-at" faults are checked on the combinational circuitry. The vector sets produce 100% Test Confidence Levels (TCL's). Since the sets are exhaustive, the vectors will test any implementation of the subject devices as long as they are functionally identical to Vendor A's devices. Tables 9-1, 9-2 and 9-3 show functional testing requirements for these devices.

3260 Test

Test programs were developed for a Tektronix 3260 automatic tester. These programs functionally test the devices by applying the sets of input vectors described above to the devices and checking the resulting output states against the expected output vectors. They also test for leakage while the bus and/or receiver outputs are in the high impedance state. While these programs were generated specifically for the 2915, 2916, and 2917 devices they may also be used for the 2905, 2906 and 2907 devices, respectively, if pull-up resistor loads are included on the open-collector bus outputs and the test program is modified to disconnect the loads during high impedance leakage measurements. Appendix D contains the wiring lists for the socket cards, copies of the test programs, pin assignment programs, and test pattern files.

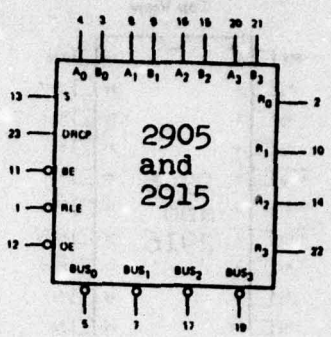
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

(A)

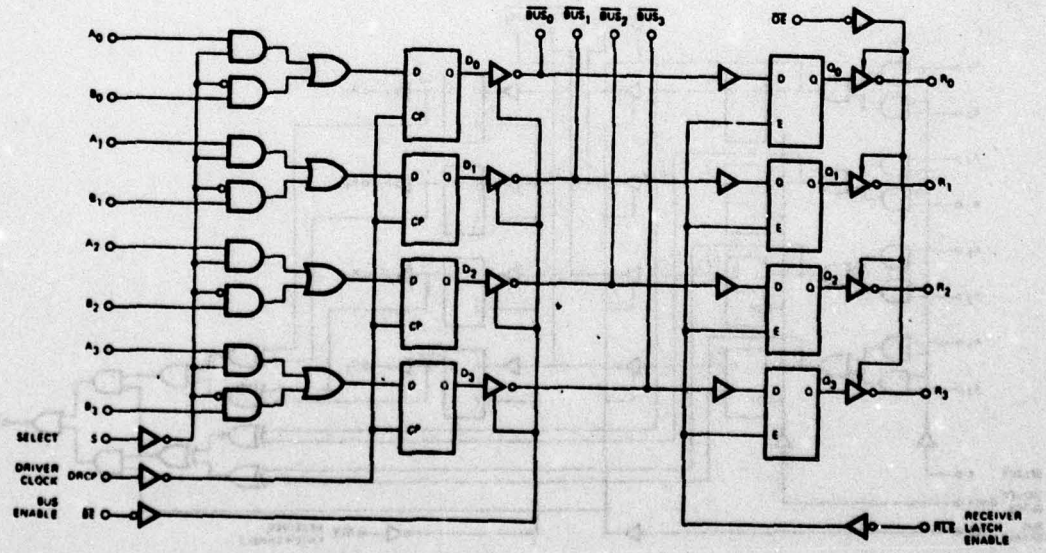
LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

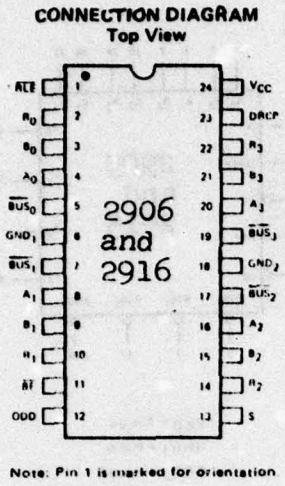
(B)

LOGIC DIAGRAM

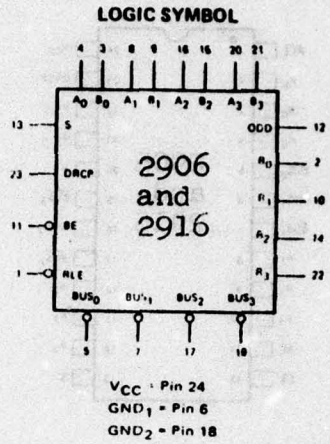


(C)

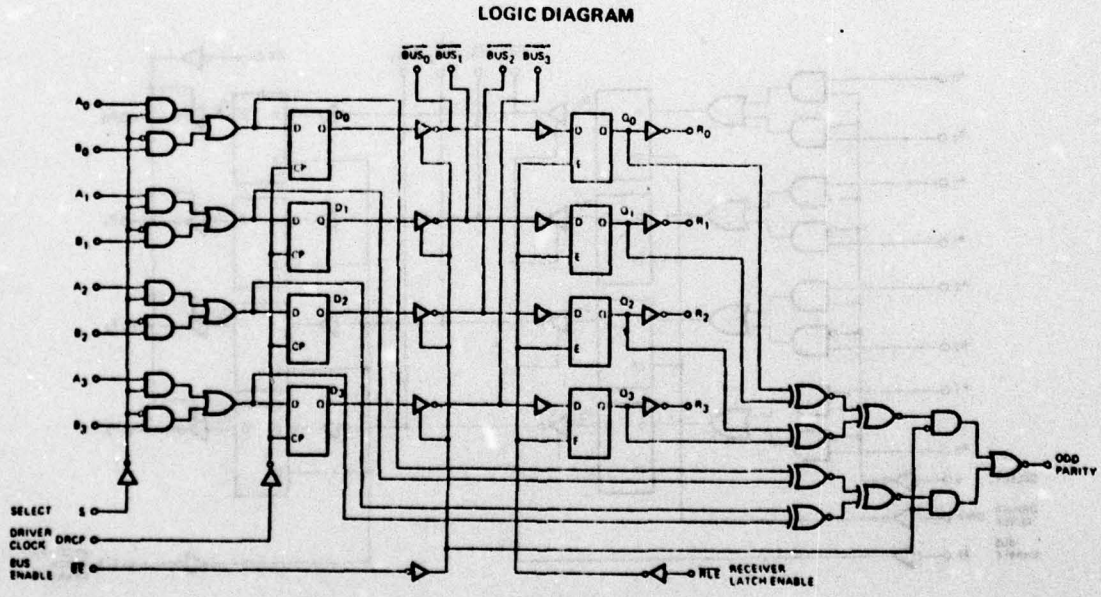
2905 and 2915 - QUAD Bus Transceiver with Interface Logic
Figure 9-1.



(A)



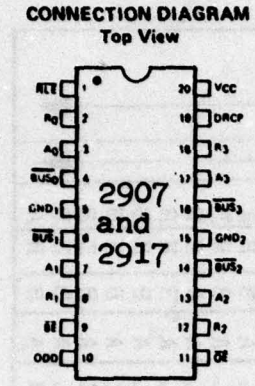
(B)



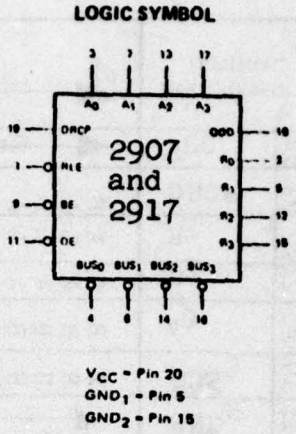
(C)

2906 and 2916 - QUAD Bus Transceiver with Interface Logic

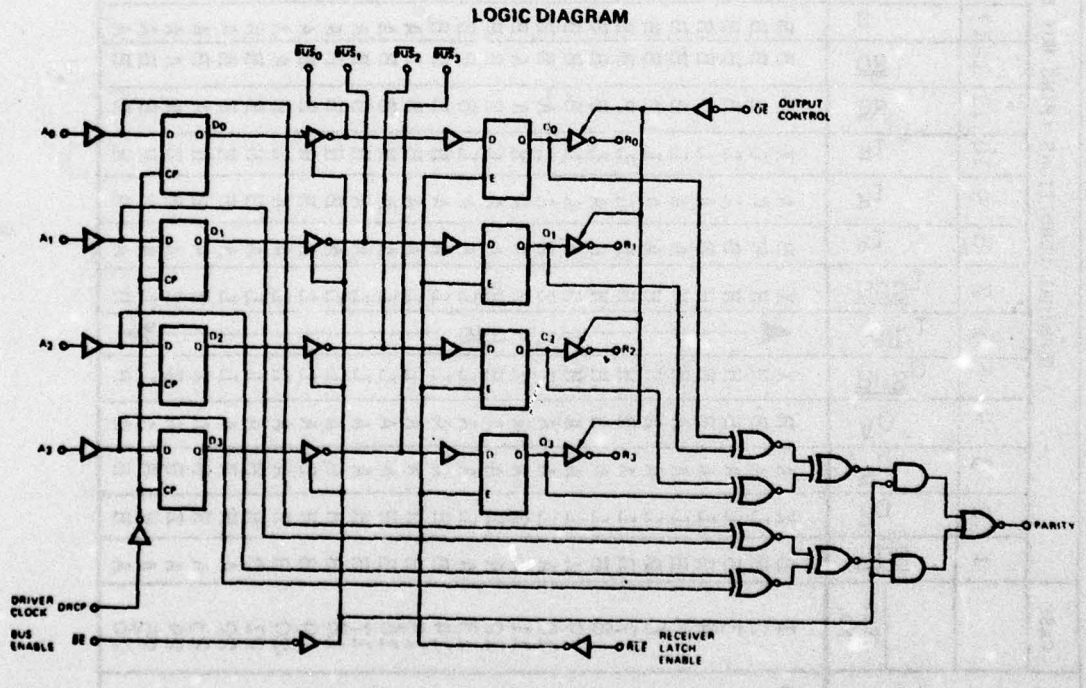
Figure 9-2.



(A)



(B)



(C)

2907 and 2917 - QUAD Bus Transceiver with Interface Logic

Figure 9-3.

Table 9-1. Functional test for the 2915, 2905

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																					MEASUREMENT TERMINAL
				TEST NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
					$\overline{RLE}$	R_0	B_0	A_0	$\overline{BUS}_0$	GND_1	$\overline{BUS}_1$	A_1	B_1	R_1	$\overline{BE}$	$\overline{OE}$	S	R_2	B_2	A_2	$\overline{BUS}_2$	GND_2	$\overline{BUS}_3$	A_3	B_3	R_3	DRCP	V_{CC}
7	Functional Test	3014		1	B	X	A	B	X	GND	X	B	A	X	B	B	B	X	A	B	X	GND	X	B	A	X	B	4.5V
				2	B	L	A	B	L		H	B	A	L	B	B	B	L	A	B	H		H	B	A	L	A	
				3	B	L	A	B	L		H	B	A	L	B	B	B	L	A	B	H		H	B	A	L	B	
				4	B	L	A	A	H		H	A	A	L	B	B	B	L	A	A	H		H	A	A	L	A	
				5	B	L	A	A	H		H	A	A	L	B	B	B	L	A	A	H		H	A	A	L	B	
				6	B	L	A	B	H		H	A	A	L	B	B	B	L	A	B	H		H	B	A	L	A	
				7	B	L	A	B	H		H	A	A	L	B	B	B	L	A	B	H		H	B	A	L	B	
				8	B	L	A	B	L		L	A	A	L	B	B	B	L	A	B	L		L	B	A	L	A	
				9	B	L	A	B	L		L	A	A	L	B	B	B	L	A	B	L		L	B	A	L	B	
				10	A	L	A	B	L		L	A	A	L	B	B	B	L	A	B	L		L	B	A	L	A	
				11	A	L	A	B	L		L	A	A	L	B	B	B	L	A	B	L		L	B	A	L	B	
				12	A	L	A	A	L		L	A	A	L	A	B	B	L	A	A	L		L	A	A	L	A	
				13	A	L	A	A	L		L	A	A	L	A	B	B	L	A	A	L		L	A	A	L	B	
				14	A	L	A	B	L		L	A	A	L	B	B	B	L	A	B	L		L	B	A	L	A	
				15	A	L	A	B	L		L	A	A	L	B	B	B	L	A	B	L		L	B	A	L	B	
				16	A	Z	A	B	Z		Z	A	A	Z	B	B	B	Z	A	B	Z		Z	B	A	Z	A	
				17	A	H	A	B	L		L	A	A	H	B	B	B	H	A	B	L		L	B	A	H	B	
				18	A	H	A	A	H		H	A	A	H	B	B	B	H	A	A	H		H	A	A	H	A	
				19	A	H	A	A	H		H	A	A	H	B	B	B	H	A	A	H		H	A	A	H	B	
				20	A	H	A	B	H		H	A	A	H	B	B	B	H	A	B	H		H	B	A	H	A	
				21	A	H	A	B	H		H	A	A	H	B	B	B	H	A	B	H		H	B	A	H	B	
				22	B	Z	A	A	L		L	A	B	Z	A	A	A	Z	B	A	L		L	A	B	Z	A	
				23	B	H	A	A	L		L	A	B	H	A	B	B	H	B	A	L		L	A	B	H	A	
				24	B	H	A	A	L		L	A	B	H	A	B	B	H	B	A	L		L	A	B	H	B	
				25	A	H	A	B	L		L	A	B	H	B	A	A	H	B	B	L		L	B	B	H	A	
				26	A	H	A	B	H		H	A	B	H	B	A	A	H	B	B	H		H	B	B	H	B	
					A11 Outputs																						

Table 9-1. - (Continued)

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																				
					1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				TEST NO.	$\overline{RLE}$	R_O	B_O	A_O	$\overline{BUS}_O$	GND_1	$\overline{BUS}_1$	A_1	B_1	R_1	$\overline{BE}$	$\overline{OE}$	S	R_2	B_2	A_2	$\overline{BUS}_2$	GND_2	$\overline{BUS}_3$	A_3
7	Functional Test	3014		27	A	H	A	B	H	GND	H	B	A	H	B	B	B	H	A	B	H	GND	H	B
				28	A	H	A	B	H		H	B	A	H	B	B	B	H	A	B	H		H	B
				29	B	L	A	B	H		H	B	A	L	B	B	A	L	A	B	H		H	B
				30	A	L	A	B	L		L	A	B	L	B	B	A	L	A	B	L		L	B
				31	A	H	B	A	H		H	A	B	H	B	B	A	H	B	B	L		L	B
				32	B	H	B	A	L		L	A	B	H	B	B	A	H	B	B	L		L	B
				33	B	L	A	B	H		H	B	A	L	B	B	A	L	A	B	L		L	B
				34	B	L	A	B	L		L	B	A	L	B	B	A	L	A	B	L		L	B
				35	B	H	A	B	H		H	B	A	H	B	B	A	H	B	B	L		L	B
				36	B	L	A	B	H		H	B	A	L	B	B	A	L	A	B	L		L	B
				37	B	H	B	A	L		L	A	B	H	B	B	A	H	B	B	L		L	B
				38	B	L	A	B	L		L	B	A	L	B	B	A	L	A	B	L		L	B
				39	B	H	A	B	H		H	B	A	H	B	B	A	H	B	B	L		L	B
				40	B	L	A	B	H		H	B	A	L	B	B	A	L	A	B	L		L	B
				41	B	H	B	A	L		L	A	B	H	B	B	A	H	B	B	L		L	B
				42	B	L	A	B	L		L	B	A	L	B	B	A	L	A	B	L		L	B
				43	B	H	A	B	H		H	B	A	H	B	B	A	H	B	B	L		L	B
				44	B	L	A	B	H		H	B	A	L	B	B	A	L	A	B	L		L	B
				45	B	H	B	A	L		L	A	B	H	B	B	A	H	B	B	L		L	B
				46	B	L	A	B	L		L	B	A	L	B	B	A	L	A	B	L		L	B
				47	B	H	A	B	H		H	B	A	H	B	B	A	H	B	B	L		L	B
				48	A	H	B	A	H		H	A	B	H	A	A	A	H	B	A	H		H	A
				49	A	H	B	A	H		H	A	B	H	A	A	A	H	B	A	H		H	A
				50	A	Z	B	A	Z		Z	A	B	Z	A	A	A	Z	B	A	Z		Z	A
				51	A	Z	B	A	Z		Z	A	B	Z	A	A	A	Z	B	A	Z		Z	A
				52	A	H	B	A	H		H	A	B	H	A	A	A	H	B	A	H		H	A
				53	A	Z	B	A	Z		Z	A	B	Z	A	A	A	Z	B	A	Z		Z	A
				54	A	Z	B	A	Z		Z	B	A	Z	B	A	B	Z	A	B	Z		Z	B
				55	A	H	B	A	H		H	B	A	L	B	A	B	L	A	B	Z		H	B

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																				
					21	22	23	24																
				TEST NO.	B_3	R_3	DRCP	V_{CC}	MEASUREMENT TERMINAL															
7	Functional Test	3014		27	A	H	B	4.5V	All Outputs															
				28	A	H	B																	
				29	A	L	B																	
				30	A	L	B																	
				31	B	H	B																	
				32	B	H	B																	
				33	A	L	B																	
				34	A	L	B																	
				35	B	H	B																	
				36	A	L	B																	
				37	B	H	B																	
				38	A	L	B																	
				39	B	H	B																	
				40	A	L	B																	
				41	B	H	B																	
				42	A	L	B																	
				43	B	H	B																	
				44	A	L	B																	
				45	B	H	B																	
				46	A	L	B																	
				47	B	H	B																	
				48	A	H	B																	
				49	A	H	B																	
				50	A	Z	B																	
				51	A	Z	B																	
				52	A	H	B																	
				53	A	Z	B																	
				54	B	Z	A																	
				55	B	H	A																	

Table 9-1. - (Continued)

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE / TEST NO.	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																								
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	MEASUREMENT TERMINAL
				$\overline{RLE}$	R_0	B_0	A_0	$\overline{BUS_0}$	GND_1	$\overline{BUS_1}$	A_1	B_1	R_1	$\overline{BE}$	$\overline{OE}$	S	R_2	B_2	A_2	$\overline{BUS_2}$	$\overline{GND_2}$	$\overline{BUS_3}$	A_3	B_3	R_3	DRCP	V_{CC}	
7 ↓	Functional Test	3014 ↓	56	B	X	B	B		↑		B	B	X	A	B	B	X	B	B		↑		B	B	X	B	↑	All Outputs
			57	B	H	B	B	B		B	B	B	H	A	B	B	H	B	B	B		B	B	B	H	B		
			58	B	L	B	B	A	GND	A	B	B	L	A	B	B	L	B	B	A	GND	A	B	B	L	B	4.5V	
			59	B	H	B	B	B		B	B	B	H	A	B	B	H	B	B	B		B	B	B	H	B		

NOTES:

1. Tests must be performed in the sequence shown above.
2. L = 0.4V Max H = 2.4V Min
3. A = 2.0V B = 0.7V for 2905, 0.8V for 2915
4. X = Don't Care
5. Z = High Impedance State - The maximum current into or out of the disabled outputs shall be as shown below.

DEVICE TYPE	01		04	
V_{OUT}	0.4V	2.4V	0.4V	2.4V
$R_3 - R_0$	± 20 uA	± 20 uA	± 20 uA	± 20 uA
$B_3 - B_0$	-50 uA	200 uA	-200 uA	50 uA

Table 9-2. Functional test for the 2916, 2906

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE / TEST NO.	1 $\overline{RLE}$	2 R_0	3 B_0	4 A_0	5 $\overline{BUS_0}$	6 GND_1	7 $\overline{BUS_1}$	8 A_1	9 B_1	10 R_1	11 $\overline{BE}$	12 ODD	13 S	14 R_2	15 B_2	16 A_2	17 $\overline{BUS_2}$	18 GND_2	19 $\overline{BUS_3}$	20 A3	21 B3	22 R_3	23 DRCP	24 V_{CC}	MEASUREMENT TERMINAL
7	Functional Test	3014	1	B	X	A	B	X	GND	X	B	A	X	B	L	B	X	A	B	X	GND	X	B	A	X	B	4.5V	All Outputs
			2	B	L	A	B	H		H	B	A	L	B	L	B	L	A	B	H		H	B	A	L	A		
			3	B	L	A	B	H		H	B	A	L	B	L	B	L	A	B	H		H	B	A	L	B		
			4	B	L	A	A	H		H	A	A	L	B	H	B	L	A	A	H		H	B	A	L	B		
			5	B	L	A	B	H		H	A	A	L	B	H	B	L	A	A	H		H	A	A	L	B		
			6	B	L	A	A	H		H	A	A	L	B	L	B	L	A	B	H		H	B	A	L	B		
			7	B	H	A	A	L		L	A	A	H	B	L	B	L	A	B	H		H	B	A	L	A		
			8	A	H	A	A	L		L	A	A	H	B	L	B	L	A	B	H		H	B	A	L	A		
			9	A	H	A	A	Z		Z	A	A	H	A	L	B	L	A	B	Z		Z	B	A	L	A		
			10	B	H	A	A	L		L	A	A	H	B	L	B	L	A	B	H		H	B	A	L	A		
			11	B	H	A	A	L		L	A	A	H	B	L	B	L	A	B	H		H	B	A	L	B		
			12	B	H	A	A	L		L	B	A	H	B	L	B	L	A	A	H		H	B	A	L	B		
			13	B	H	A	A	L		H	B	A	L	B	L	B	H	A	A	L		H	B	A	L	A		
			14	A	H	A	A	L		H	B	A	L	B	L	B	H	A	A	L		H	B	A	L	A		
			15	A	H	A	A	Z		Z	B	A	L	A	L	B	H	A	A	Z		Z	B	A	L	A		
			16	B	H	A	A	L		H	B	A	L	B	L	B	H	A	A	L		H	B	A	L	A		
			17	B	H	A	A	L		H	B	A	L	B	L	B	H	A	A	L		H	B	A	L	B		
			18	B	H	A	B	L		H	B	A	L	B	H	B	H	A	B	L		H	B	A	L	B		
			19	B	L	A	B	H		H	B	A	L	B	H	B	L	A	B	H		L	A	A	H	A		
			20	A	L	A	B	H		H	B	A	L	B	H	B	L	A	B	H		L	A	A	H	A		
			21	A	L	A	B	Z		Z	B	A	L	A	H	B	L	A	B	Z		Z	A	A	H	A		
			22	B	L	A	B	H		H	B	A	L	B	H	B	L	A	B	H		L	A	A	H	A		
			23	B	L	A	B	H		H	B	A	L	B	H	B	L	A	B	H		L	A	A	H	B		
			24	B	L	B	A	H		H	A	A	L	B	H	A	L	A	A	H		L	A	A	H	B		
			25	B	L	B	A	H		L	A	A	H	B	H	A	H	A	A	L		L	A	A	H	A		
			26	A	L	B	A	H		L	A	A	H	B	H	A	H	A	A	L		L	A	A	H	A		

TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)

Table 9-2. - (Continued)

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE / TEST NO.	1 $\overline{RLE}$	2 R_0	3 B_0	4 A_0	5 $\overline{BUS}_0$	6 GND_1	7 $\overline{BUS}_1$	8 A_1	9 B_1	10 R_1	11 $\overline{BE}$	12 ODD	13 S	14 R_2	15 B_2	16 A_2	17 $\overline{BUS}_2$	18 GND_2	19 $\overline{BUS}_3$	20 A_3	21 B_3	22 R_3	23 DRCP	24 V_{CC}	MEASUREMENT TERMINAL
7	Functional Test	3014	27	A	L	B	A	Z	GND	Z	A	A	H	A	H	A	H	A	A	Z	GND	Z	A	A	H	A	4.5V	All Outputs
			28	A	L	A	A	Z		Z	A	A	H	A	H	A	H	A	A	Z		Z	A	A	H	A		
			29	A	L	B	A	H		L	A	A	H	B	H	A	H	A	A	L		L	A	A	H	A		
			30	A	L	A	A	H		L	A	B	H	B	H	A	H	B	A	L		L	A	B	H	A		
			31	A	L	A	A	H		L	A	B	H	B	H	A	H	B	A	L		L	A	B	H	B		
			32	A	L	A	A	L		H	A	B	H	B	H	A	H	B	A	H		H	A	B	H	A		
			33	B	H	A	A	L		H	A	B	L	B	H	A	L	B	A	H		H	A	B	L	A		
			34	A	H	B	A	L		H	A	A	L	B	H	A	L	A	A	H		H	A	A	L	A		
			35	A	H	B	A	L		H	A	A	L	B	H	A	L	A	A	H		H	A	A	L	B		
			36	A	H	B	A	H		L	A	A	L	B	H	A	L	A	A	L		L	A	A	L	A		
			37	B	L	B	A	H		L	A	A	H	B	H	A	H	A	A	L		L	A	A	H	B		
			38	A	L	B	A	H		L	A	A	H	B	L	A	H	A	A	L		L	A	B	H	B		
			39	A	L	B	A	H		L	A	A	H	B	L	A	H	A	A	L		H	A	B	H	A		
			40	A	L	A	B	H		L	A	B	H	B	L	B	H	B	A	L		H	B	A	H	B		
			41	A	L	A	B	H		L	A	B	H	B	L	B	H	B	A	L		H	B	A	H	A		
			42	B	L	B	A	H		L	A	B	H	B	L	A	H	A	B	L		H	B	A	L	B		
			43	B	L	B	A	H		H	A	B	L	B	L	A	H	A	B	L		L	B	A	H	A		
			44	A	L	A	B	H		H	B	A	L	B	H	A	H	B	A	L		L	B	A	H	B		
			45	A	L	A	B	L		L	B	A	L	B	H	A	H	B	A	H		L	B	A	H	A		
			46	A	L	A	B	Z		Z	B	A	L	A	L	B	H	A	B	Z		Z	B	A	H	B		
			47	A	L	A	B	Z		Z	B	A	L	A	L	B	H	A	B	Z		Z	B	A	H	A		
			48	B	L	A	B	H		H	B	A	L	B	L	B	L	A	B	H		H	B	A	L	A		
			49	A	L	B	A	H		H	A	B	L	B	L	A	L	B	A	H		H	A	B	L	B		
			50	A	L	B	A	Z		Z	A	B	L	A	L	A	L	B	A	Z		Z	A	B	L	B		
			51	A	L	B	A	Z		Z	A	B	L	A	L	A	L	B	A	Z		Z	A	B	L	A		
			52	B	L	A	B	H		H	B	A	L	B	L	A	L	A	B	H		H	B	A	L	B		

TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)

Table 9-2. - (Continued)

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE / TEST NO.	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																								MEASUREMENT TERMINAL
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
				$\overline{RLE}$	R_0	B_0	A_0	$\overline{BUS}_0$	GND_1	$\overline{BUS}_1$	A_1	B_1	R_1	$\overline{BE}$	ODD	S	R_2	B_2	A_2	$\overline{BUS}_2$	GND_2	$\overline{BUS}_3$	A_3	B_3	R_3	DRCP	V_{CC}	
7	Functional Test	3014	53	B	H	A	B	L	GND	L	B	A	H	B	L	A	H	A	B	L	GND	L	B	A	H	A	4.5V	All Outputs
			54	A	H	B	A	L		L	A	B	H	B	L	A	H	B	A	L		L	A	B	H	B		
			55	A	H	B	A	H		H	A	B	H	B	L	A	H	B	A	H		H	A	B	H	A		
			56	A	H	B	A	H		H	A	B	H	B	L	B	H	B	A	H		H	A	B	H	B		
			57	A	H	B	A	L		L	A	B	H	B	L	B	H	B	A	L		L	A	B	H	A		
			58	A	H	B	A	L		L	A	B	H	B	H	B	H	B	A	L		L	B	A	H	B		
			59	A	H	B	A	L		L	A	B	H	B	H	B	H	B	A	L		H	B	A	H	A		
			60	B	X	B	B				B	B	X	A	X	B	X	B	B				B	B	X	B		
			61	B	H	B	B	B		B	B	B	H	A	L	B	H	B	B	B		B	B	B	H	B		
			62	B	L	B	B	A		A	B	B	L	A	L	B	L	B	B	A		A	B	B	L	B		
			63	B	H	B	B	B		B	B	B	H	A	L	B	H	B	B	B		B	B	B	H	B		

NOTES:

1. Tests must be performed in the sequence shown above.
2. L = 0.4V Max H = 2.4V Min
3. A = 2.0V B = 0.7V for 2906, 0.8V for 2916
4. X = Don't Care
5. Z = High Impedance State - The maximum current into or out of the disabled outputs shall be as shown below.

DEVICE TYPE	02		05	
V_{OUT}	0.4V	2.4V	0.4V	2.4V
B_3 - B_0	-50 uA	200 uA	-200 uA	50 uA

Table 9-3. Functional test for the 2917, 2907

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE / TEST NO.	1 $\overline{RLE}$	2 R_0	3 A_0	4 $\overline{BUS_0}$	5 GND_1	6 $\overline{BUS_1}$	7 A_1	8 R_1	9 $\overline{BE}$	10 ODD	11 $\overline{OE}$	12 R_2	13 A_2	14 $\overline{BUS_2}$	15 GND_2	16 $\overline{BUS_3}$	17 A_3	18 R_3	19 DRCP	20 V_{CC}	21	22	23	24	MEASUREMENT TERMINAL
7	Functional Test	3014	1	B	X	B	X	GND	X	B	X	B	L	B	X	B	X	GND	X	B	X	B	4.5V					All Outputs
			2	B	L	B	H		H	B	L	B	L	B	L	B	H		H	B	L	A						
			3	B	L	B	H		H	B	L	B	L	B	L	B	H		H	B	L	B						
			4	B	L	A	H		H	A	L	B	H	B	L	A	H		H	B	L	B						
			5	B	L	B	H		H	A	L	B	H	B	L	A	H		H	A	L	B						
			6	B	L	A	H		H	A	L	B	L	B	L	B	H		H	B	L	B						
			7	B	H	A	L		L	A	H	B	L	B	L	B	H		H	B	L	A						
			8	A	H	A	L		L	A	H	B	L	B	L	B	H		H	B	L	A						
			9	A	H	A	Z		Z	A	H	A	L	B	L	B	Z		Z	B	L	A						
			10	A	Z	A	Z		Z	A	Z	A	L	A	Z	B	Z		Z	B	Z	A						
			11	B	H	A	L		L	A	H	B	L	B	L	B	H		H	B	L	A						
			12	B	H	A	L		L	A	H	B	L	B	L	B	H		H	B	L	B						
			13	B	H	A	L		L	B	H	B	L	B	L	A	H		H	B	L	B						
			14	B	H	A	L		H	B	L	B	L	B	H	A	L		H	B	L	A						
			15	A	H	A	L		H	B	L	B	L	B	H	A	L		H	B	L	A						
			16	A	H	A	Z		Z	B	L	A	L	B	H	A	Z		Z	B	L	A						
			17	A	Z	A	Z		Z	B	Z	A	L	A	Z	A	Z		Z	B	Z	A						
			18	B	H	A	L		H	B	L	B	L	B	H	A	L		H	B	L	A						
			19	B	H	A	L		H	B	L	B	L	B	H	A	L		H	B	L	B						
			20	B	H	B	L		H	B	L	B	H	B	H	B	L		H	A	L	B						
			21	B	L	B	H		H	B	L	B	H	B	L	B	H		L	A	H	A						
			22	A	L	B	H		H	B	L	B	H	B	L	B	H		L	A	H	A						
			23	A	L	B	Z		Z	B	L	A	H	B	L	B	Z		Z	A	H	A						
			24	A	Z	B	Z		Z	B	Z	A	H	A	Z	B	Z		Z	A	Z	A						
			25	B	L	B	H		H	B	L	B	H	B	L	B	H		L	A	H	A						
			26	B	L	B	H		H	B	L	B	H	B	L	B	H		L	A	H	A						

TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)

Table 9-3. - (Continued)

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																					MEASUREMENT TERMINAL
				TEST NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
7	Functional Test	3014		27	B	L	B	H	GND	H	A	L	B	H	B	L	A	H	GND	L	A	H	B	V_{CC}				
				28	B	L	B	H		L	A	H	B	H	B	H	A	Z		L	A	H	A	4.5V				
				29	A	L	A	L		Z	A	H	B	H	B	H	A	Z		Z	A	H	A					
				30	A	L	A	L		Z	A	H	B	H	B	H	A	L		L	A	H	A					
				31	A	L	A	L		L	A	H	B	H	B	H	A	L		L	A	H	A					
				32	A	L	A	L		L	A	H	B	H	B	H	A	H		H	A	H	A					
				33	A	L	A	L		H	A	H	B	H	B	H	A	H		H	A	H	A					
				34	A	H	A	H		H	A	H	B	H	B	H	A	H		H	A	H	A					
				35	B	L	B	L		L	A	L	B	H	B	H	A	H		H	B	H	A					
				36	A	L	A	L		L	A	L	B	H	B	H	A	L		L	A	H	A					
				37	A	L	A	L		Z	A	H	B	H	B	H	A	L		L	A	H	A					
				38	A	L	A	L		Z	A	H	B	H	B	H	A	H		H	A	H	A					
				39	A	H	A	H		H	A	H	B	H	B	H	A	H		H	A	H	A					
				40	B	L	B	L		L	A	L	B	H	B	H	A	H		H	B	H	A					
				41	A	L	A	L		L	A	L	B	H	B	H	A	L		L	A	H	A					
				42	A	L	A	L		Z	A	H	B	H	B	H	A	L		L	A	H	A					
				43	A	L	A	L		Z	A	H	B	H	B	H	A	H		H	A	H	A					
				44	A	H	A	H		H	A	H	B	H	B	H	A	H		H	A	H	A					
				45	B	L	B	L		L	A	L	B	H	B	H	A	H		H	B	H	A					
				46	B	Z	B	Z		Z	B	Z	A	L	A	L	B	Z		Z	B	Z	B					
				47	B	H	B	H		H	B	H	A	L	A	L	B	Z		Z	B	Z	B					
				48	B	Z	B	Z		Z	B	Z	A	L	A	L	B	H		H	B	L	B					
				49	B	X	B	X		X	B	X	A	L	A	L	B	H		H	B	L	B					
				50	B	H	B	H		H	B	H	A	L	A	L	B	H		H	B	L	B					
				51	B	L	B	L		L	A	L	B	H	B	H	A	H		H	B	H	A					
				52	B	H	B	H		L	A	L	B	H	B	H	A	H		H	B	H	A					

Table 9-3.

NOTES:

1. Tests must be performed in the sequence shown above.
2. L = 0.4V Max H = 2.4V Min
3. A = 2.0V B = 0.7V for 2707, 0.8V for 2917
4. X = Don't Care
5. Z = High Impedance State - The maximum current into or out of the disabled outputs shall be as shown below.

DEVICE TYPE	03		06	
V_{OUT}	0.4V	2.4V	0.4V	2.4V
R_3 - R_0	$\pm$20 µA	$\pm$20 µA	$\pm$20 µA	$\pm$20 µA
B_3 - B_0	-50 µA	200 µA	-200 µA	50 µA

APPENDIX A

ADDITIONS AND CHANGES MADE TO THE

PROPOSED MIL-M-38510/440

NOTE: Table and Figure references in this appendix are numbered in accordance with the MIL-38510/440 Draft numbering so that ready reference is possible. Certain tables and figures have been omitted.

i. Additions to Table I

Table I in the preliminary slash sheet contained only the DC parameters for the 2901A. The following pages, which contain all of the AC parameters for the 2901A, were added to the slash sheet by General Electric.

TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS

TEST	SYMBOL	CONDITIONS	WAVEFORM FIGURE	LIMITS		UNITS
				MIN.	MAX.	
Delay from A_3-A_0 to Y_3-Y_0	t_{PHL1}	R_L = 68Ω	7		90	ns
	t_{PLH1}	R = 1.5KΩ	7		90	ns
		Y_3-Y_0, G				
Delay from A_3-A_0 to F_3	t_{PHL2}		7		80	ns
	t_{PLH2}	R_L = 110Ω	7		80	ns
		R = 2.4KΩ				
Delay from A_3-A_0 to C_{n+4}	t_{PHL3}	C_{n+4}	7		80	ns
	t_{PLH3}		7		80	ns
		R_L = 140Ω				
Delay from A_3-A_0 to $\overline{G}$ and $\overline{P}$	t_{PHL4}	R = 3.0KΩ	7		80	ns
	t_{PLH4}	OVR, P	7		80	ns
Delay from A_3-A_0 to F=0	t_{PHL5}	R_L = 250Ω	7		90	ns
	t_{PLH5}	R = 4.8KΩ	7		90	ns
		F3, RAM3.0, Q3.0				
Delay from A_3-A_0 to OVR	t_{PHL6}		7		90	ns
	t_{PLH6}	R_L = 316Ω	7		90	ns
		F = 0 device				
Delay from A_3-A_0 to RAM_3 and RAM_0	t_{PHL7}	type 01	7		100	ns
	t_{PLH7}		7		100	ns
		R_L = 510Ω				
Delay from B_3-B_0 to Y_3-Y_0	t_{PHL8}	F = 0 device	7		90	ns
	t_{PLH8}	type 02	7		90	ns
Delay from B_3-B_0 to F_3	t_{PHL9}	C_L = 50 pF ± 5 pF	7		80	ns
	t_{PLH9}	all outputs	7		80	ns
Delay from B_3-B_0 to C_{n+4}	t_{PHL10}		7		80	ns
	t_{PLH10}		7		80	ns
Delay from B_3-B_0 to $\overline{G}$ and $\overline{P}$	t_{PHL11}		7		80	ns
	t_{PLH11}		7		80	ns
Delay from B_3-B_0 to F=0	t_{PHL12}		7		90	ns
	t_{PLH12}		7		90	ns
Delay from B_3-B_0 to OVR	t_{PHL13}		7		90	ns
	t_{PLH13}		7		90	ns
Delay from B_3-B_0 to RAM_3 and RAM_0	t_{PHL14}		7		100	ns
	t_{PLH14}		7		100	ns
Delay from D_3-D_0 (ARITH) to Y_3-Y_0	t_{PHL15}		7		60	ns
	t_{PLH15}		7		60	ns
Delay from D_3-D_0 (ARITH) to F_3	t_{PHL16}		7		50	ns
	t_{PLH16}		7		50	ns

TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS (CONT'D.)

TEST	SYMBOL	CONDITIONS	WAVEFORM FIGURE	LIMITS MIN	LIMITS MAX.	UNITS
Delay from D_3-D_0 (ARITH) to C_{n+4}	t_{PHL17}	R_L = 68Ω	7		50	ns
	t_{PLH17}	R = 1.5KΩ	7		50	ns
		Y_3-Y_0, G				
Delay from D_3-D_0 (ARITH) to $\overline{G}$ and $\overline{P}$	t_{PHL18}		7		50	ns
	t_{PLH18}	R_L = 110Ω	7		50	ns
		R = 2.4KΩ				
Delay from D_3-D_0 (ARITH) to F=0	t_{PHL19}	C_{n+4}	7		60	ns
	t_{PLH19}		7		60	ns
		R_L = 140Ω				
Delay from D_3-D_0 (ARITH) to OVR	t_{PHL20}	R = 3.0KΩ	7		60	ns
	t_{PLH20}	OVR, P	7		60	ns
Delay from D_3-D_0 (ARITH) to RAM_3 and RAM_0	t_{PHL21}	R_L = 250Ω	7		70	ns
	t_{PLH21}	R = 4.8KΩ	7		70	ns
		F3, RAM3.0, Q3.0				
Delay from D_3-D_0 (I = X37) to Y_3-Y_0	t_{PHL22}		7		60	ns
	t_{PLH22}	R_L = 316Ω	7		60	ns
		F = 0 device				
Delay from D_3-D_0 (I = X37) to F_3	t_{PHL23}	type 01	7		50	ns
	t_{PLH23}		7		50	ns
		R_L = 510Ω				
Delay from D_3-D_0 (I = X37) to F=0	t_{PHL24}	F = 0 device	7		60	ns
	t_{PLH24}	type 02	7		60	ns
Delay from D_3-D_0 (I = X37) to RAM_3 and RAM_0	t_{PHL25}	C_L = 50 pF ± 5 pF	7		65	ns
	t_{PLH25}	all outputs	7		65	ns
Delay from C_n to Y_3-Y_0	t_{PHL26}		7		45	ns
	t_{PLH26}		7		45	ns
Delay from C_n to F_3	t_{PHL27}		7		30	ns
	t_{PLH27}		7		30	ns
Delay from C_n to C_{n+4}	t_{PHL28}		7		30	ns
	t_{PLH28}		7		30	ns
Delay from C_n to F=0	t_{PHL29}		7		50	ns
	t_{PLH29}		7		50	ns
Delay from C_n to OVR	t_{PHL30}		7		40	ns
	t_{PLH30}		7		40	ns
Delay from C_n to RAM_3 and RAM_0	t_{PHL31}		7		55	ns
	t_{PLH31}		7		55	ns

TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS (CONT'D.)

TEST	SYMBOL	CONDITIONS	WAVEFORM FIGURE	LIMITS MIN.	LIMITS MAX.	UNITS
Delay from I_2-I_0 to Y_3-Y_0	t_{PHL32}	R_L = 68Ω	7		70	ns
	t_{PLH32}	R = 1.5KΩ Y_3-Y_0, G	7		70	ns
Delay from I_2-I_0 to F_3	t_{PHL33}		7		60	ns
	t_{PLH33}	R_L = 110Ω R = 2.4KΩ	7		60	ns
Delay from I_2-I_0 to C_{n+4}	t_{PHL34}	C_{n+4}	7		60	ns
	t_{PLH34}	R_L = 140Ω	7		60	ns
Delay from I_2-I_0 to $\overline{G}$ and $\overline{P}$	t_{PHL35}	R = 3.0KΩ	7		50	ns
	t_{PLH35}	OVR, P	7		50	ns
Delay from I_2-I_0 to F=0	t_{PHL36}	R_L = 250Ω	7		70	ns
	t_{PLH36}	R = 4.8KΩ F3, RAM3,0, Q3,0	7		70	ns
Delay from I_2-I_0 to OVR	t_{PHL37}		7		70	ns
	t_{PLH37}	R_L = 316Ω F = 0 device	7		70	ns
Delay from I_2-I_0 to RAM_3 and RAM_0	t_{PHL38}	type 01	7		80	ns
	t_{PLH38}		7		80	ns
Delay from I_5-I_3 to Y_3-Y_0	t_{PHL39}	R_L = 510Ω F = 0 device	7		60	ns
	t_{PLH39}	type 02	7		60	ns
Delay from I_5-I_3 to F_3	t_{PHL40}	C_L = 50 pF ± 5 pF	7		50	ns
	t_{PLH40}	all outputs	7		50	ns
Delay from I_5-I_3 to C_{n+4}	t_{PHL41}		7		60	ns
	t_{PLH41}		7		60	ns
Delay from I_5-I_3 to $\overline{G}$, $\overline{P}$	t_{PHL42}		7		55	ns
	t_{PLH42}		7		55	ns
Delay from I_5-I_3 to F=0	t_{PHL43}		7		60	ns
	t_{PLH43}		7		60	ns
Delay from I_5-I_3 to OVR	t_{PHL44}		7		70	ns
	t_{PLH44}		7		70	ns
Delay from I_5-I_3 to RAM_3 and RAM_0	t_{PHL45}		7		80	ns
	t_{PLH45}		7		80	ns
Delay from I_8-I_6 to Y_3-Y_0	t_{PHL46}		7		45	ns
	t_{PLH46}		7		45	ns

TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS (CONT'D.)

TEST	SYMBOL	CONDITIONS	WAVEFORM FIGURE	LIMITS MIN	LIMITS MAX.	UNITS
Delay from A_3-A_0 (I = 2XX) to Y_3-Y_0	t_{PHL47}	R_L = 68Ω	7		50	ns
	t_{PLH47}	R = 1.5KΩ	7		50	ns
Delay from CP to Y_3-Y_0	t_{PHL48}	Y_3-Y_0, G	8		90	ns
	t_{PLH48}	R_L = 110Ω	8		90	ns
Delay from CP to F_3	t_{PHL49}	R = 2.4KΩ C_{n+4}	8		80	ns
	t_{PLH49}		8		80	ns
Delay from CP to C_{n+4}	t_{PHL50}	R_L = 140Ω	8		80	ns
	t_{PLH50}	R = 3.0KΩ OVR, P	8		80	ns
Delay from CP to $\overline{G}$ and $\overline{P}$	t_{PHL51}	R_L = 250Ω	8		70	ns
	t_{PLH51}	R = 4.8KΩ F3, RAM3,0, Q3,0	8		70	ns
Delay from CP to F=0	t_{PHL52}		8		90	ns
	t_{PLH52}	R_L = 316Ω F = 0 device	8		90	ns
Delay from CP to OVR	t_{PHL53}	type 01	8		80	ns
	t_{PLH53}		8		80	ns
Delay from CP to RAM_3 and RAM_0	t_{PHL54}	R_L = 510Ω F = 0 device	8		90	ns
	t_{PLH54}	type 02	8		90	ns
Delay from CP to Q_3 and Q_0	t_{PHL55}	C_L = 50 pF ± 5 pF	8		50	ns
	t_{PLH55}	all outputs	8		50	ns
Delay from $\overline{OE}$ to Y_3-Y_0 FLOAT	t_{PHZ1}		12		30	ns
	t_{PLZ1}		12		30	ns
Delay from I8-I6 to RAM_3 and RAM_0 FLOAT	t_{PHZ2}		12			ns
	t_{PLZ2}		12			ns
Delay from I8-I6 to Q_3 and Q_0 FLOAT	t_{PHZ3}		12			ns
	t_{PLZ3}		12			ns
Delay from $\overline{OE}$ to Y_3-Y_0	t_{PZL1}		12		40	ns
	t_{PZH1}		12		40	ns
Delay from I8-I6 to RAM_3 and RAM_0	t_{PZL2}		12		50	ns
	t_{PZH2}		12		50	ns
Delay from I8-I6 to Q_3 and Q_0	t_{PZL3}		12		50	ns
	t_{PZH3}		12		50	ns

TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS (CONT'D.)

TEST	SYMBOL	CONDITIONS	WAVEFORM FIGURE	LIMITS MIN.	LIMITS MAX.	UNITS
A_3-A_0 Set Up Time To Positive Edge of Clock	t_{SHL1} t_{SLH1}		9 9	110 110		ns ns
A_3-A_0 Set Up Time To Negative Edge of Clock	t_{SHL2} t_{SLH2}		9 9	30 30		ns ns
B_3-B_0 (Source) Set Up Time To Positive Edge of Clock	t_{SHL3} t_{SLH3}		9 9	110 110		ns ns
B_3-B_0 (Source) Set Up Time To Negative Edge of Clock	t_{SHL4} t_{SLH4}		9 9	30 30		ns ns
B_3-B_0 (DEST) Set Up Time to Negative Edge of Clock	t_{SHL5} t_{SLH5}		11 11	15 15		ns ns
D_3-D_0 (Arithmetic Mode) Set Up Time to Positive Edge of Clock	t_{SHL6} t_{SLH6}		10 10	75 75		ns ns
D_3-D_0 (I = X37) Set Up Time To Positive Edge of Clock	t_{SHL7} t_{SLH7}		11 11	65 65		ns ns
C_n Set Up Time to Positive Edge of Clock	t_{SHL8} t_{SLH8}		10 10	60 60		ns ns
I_2-I_0 Set Up Time to Positive Edge of Clock	t_{SHL9} t_{SLH9}		10 10	85 85		ns ns
I_5-I_3 Set Up Time to Positive Edge of Clock	t_{SHL10} t_{SLH10}		10 10	85 85		ns ns
I_8-I_6 Set Up Time to Negative Edge of Clock	t_{SHL11} t_{SLH11}		10 10	30 30		ns ns
Q_3, Q_0 Set Up Time to Positive Edge of Clock	t_{SHL12} t_{SLH12}		10 10	25 25		ns ns
RAM_3, RAM_0 Set Up Time to Positive Edge of Clock	t_{SHL13} t_{SLH13}		10 10	25 25		ns ns
A_3-A_0 Hold Time From Positive Edge of Clock	t_{HHL1} t_{HLH1}		7 7	0 0		ns ns

TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS (CONT'D.)

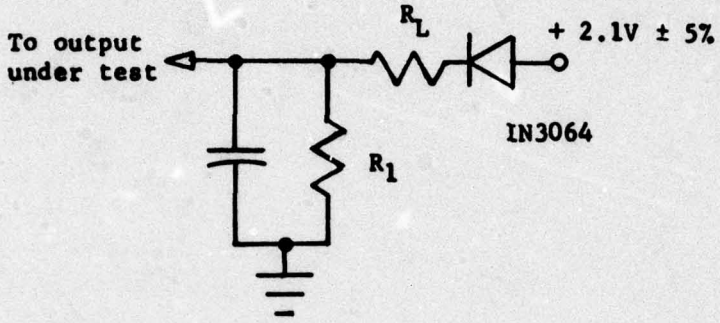
TEST	SYMBOL	CONDITIONS	WAVEFORM FIGURE	LIMITS MIN	LIMITS MAX.	UNITS
B_3-B_0 Hold Time From Positive Edge of Clock	t_{HHL2}		7	0		ns
	t_{HLH2}		7	0		ns
D_3-D_0 Hold Time From Positive Edge of Clock	t_{HHL3}		7	0		ns
	t_{HLH3}		7	0		ns
C_n Hold Time From Positive Edge of Clock	t_{HHL4}		7	0		ns
	t_{HLH4}		7	0		ns
I_8-I_0 Hold Time From Positive Edge of Clock	t_{HHL5}		7	0		ns
	t_{HLH5}		7	0		ns
Q_3, Q_0 Hold Time From Positive Edge of Clock	t_{HHL6}		10	0		ns
	t_{HLH6}		10	0		ns
RAM_3, RAM_0 Hold Time From Positive Edge of Clock	t_{HHL7}		10	0		ns
	t_{HLH7}		10	0		ns

TABLE I ELECTRICAL PERFORMANCE CHARACTERISTICS (CONT'D.)

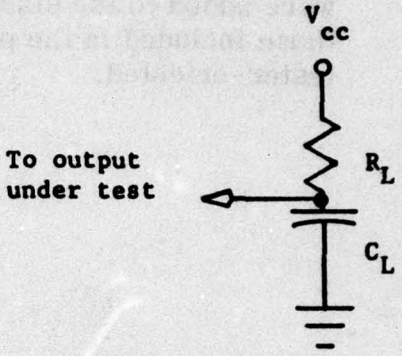
TEST	SYMBOL	CONDITIONS	WAVEFORM FIGURE	LIMITS MIN	LIMITS MAX.	UNITS
Min Clock Low Time	t_{PWL}	R_L = 68Ω R = 1.5KΩ Y_3-Y_0, G	13	30		ns
Min Clock High Time	t_{PWH}	R_L = 110Ω R = 2.4KΩ C_{n+4}	13	30		ns
Min Clock Period		R_L = 140Ω R = 3.0KΩ OVR, P	13	110		ns
Read-Modify-Write Cycle (Time from Selection of A, B Registers to End of Cycle		R_L = 250Ω R = 4.8KΩ F3, RAM3,0, Q3,0	13	110		ns
Max Clock Freq to Shift Q Register (50% Duty Cycle) I = 432 or 632		R_L = 316Ω F = 0 device type 01 R_L = 510Ω F = 0 device type 02 C_L = 50 pF ± 5 pF all outputs	13	12		MHz

ii. Revised Loads for Switching Tests

The loads on the following page were recommended by GE because they better represent what the device will see in actual use. The revised loads can be used on three-state outputs without requiring the opening and closing of switches as was necessary with the original load.



All output loads except F = 0



F = 0 Output Load

	R_L	R
Y_{3-0}, $\overline{G}$	68	1.5 K
C_n + 4	110	2.4 K
OVR, $\overline{P}$	140	3.0 K
F_3, $RAM_{3,0}$, $Q_{3,0}$	250	4.8 K

	R_L
F = 0 Device Type 01	316
F = 0 Device Type 02	510

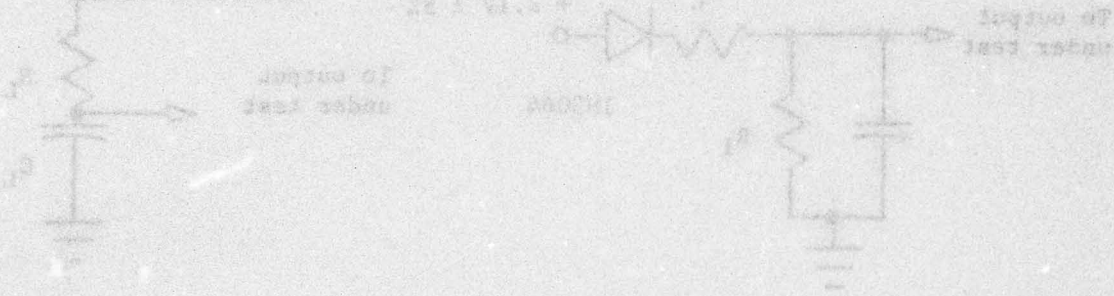
NOTES

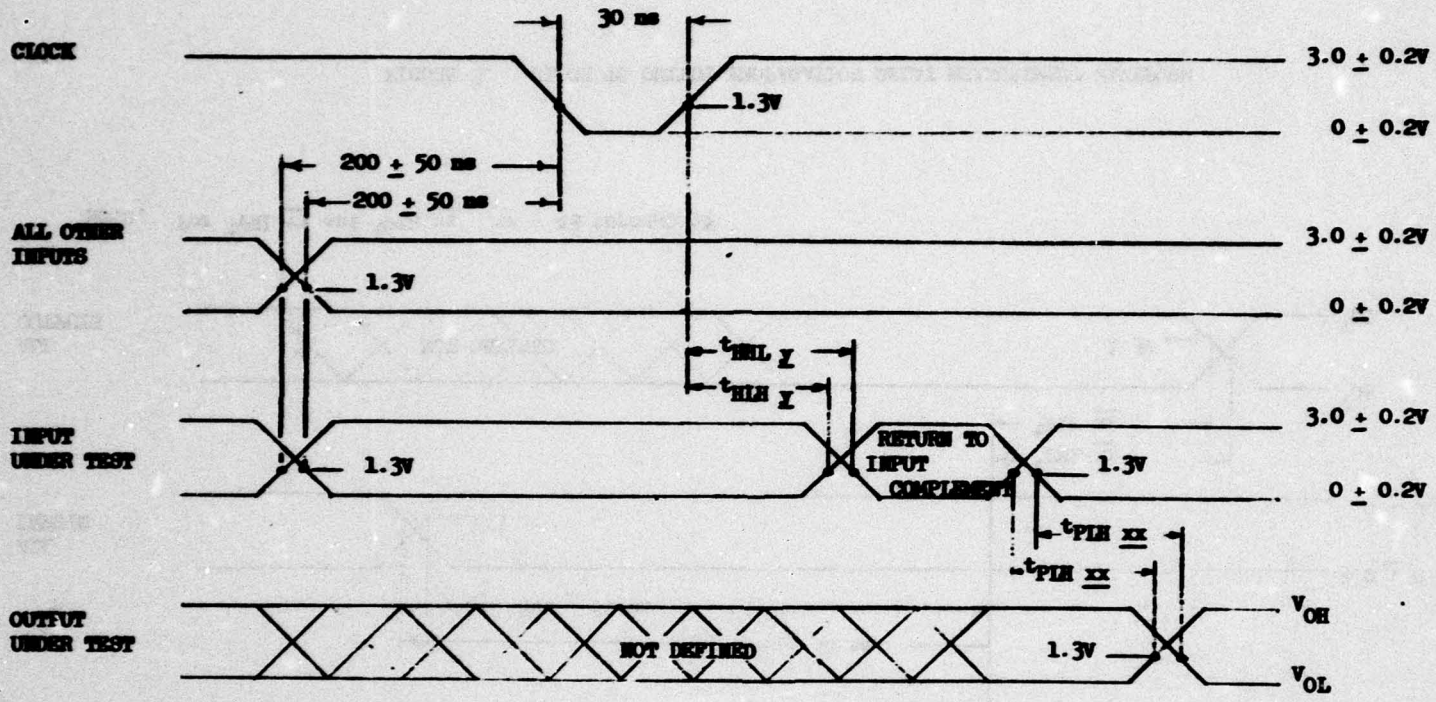
1. C_L = 50pf ± 5 pf includes scope probe, wiring and stray capacitance without device in test fixture.

Figure 6. Switching time test circuit loads

iii. Revised Timing Diagrams

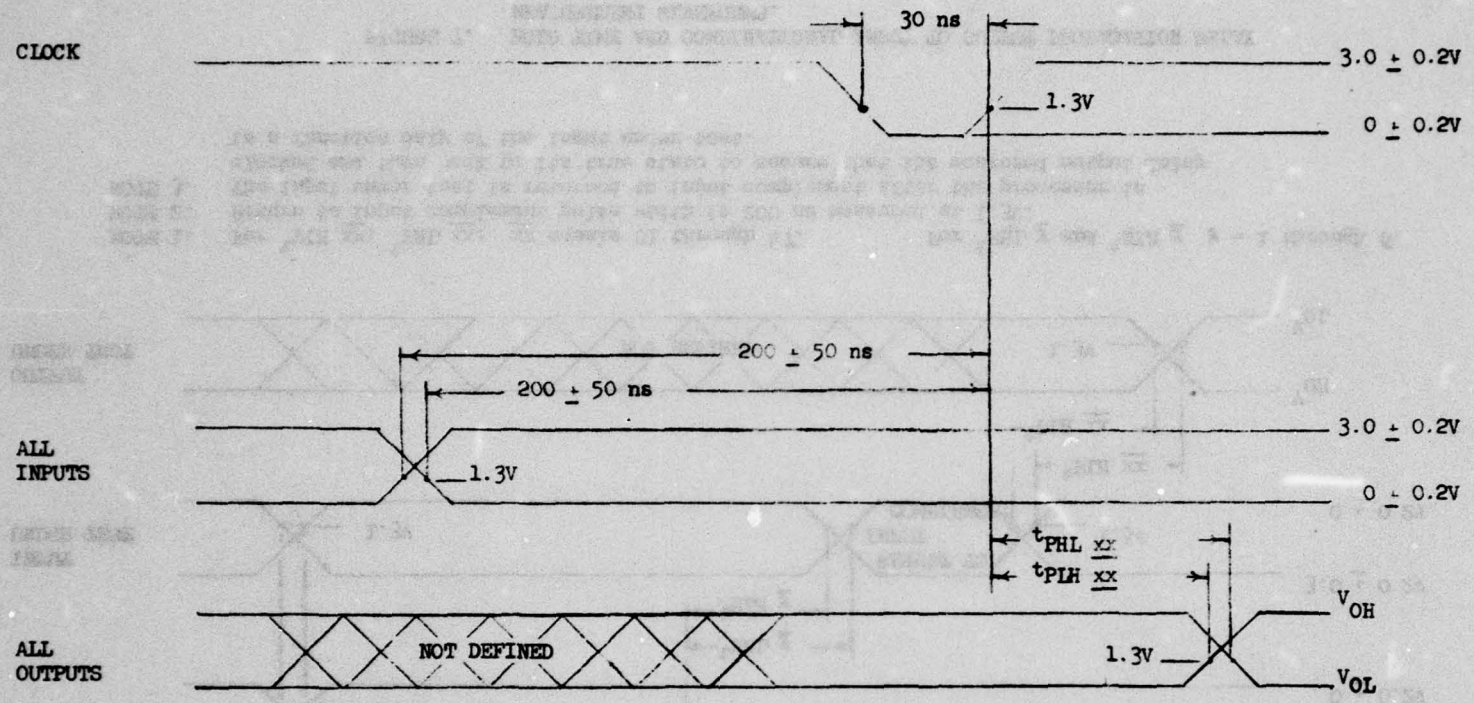
The following pages contain the revised timing diagrams which were added to the slash sheet by GE. They are clearer than those included in the preliminary slash sheet and are no longer tester-oriented.





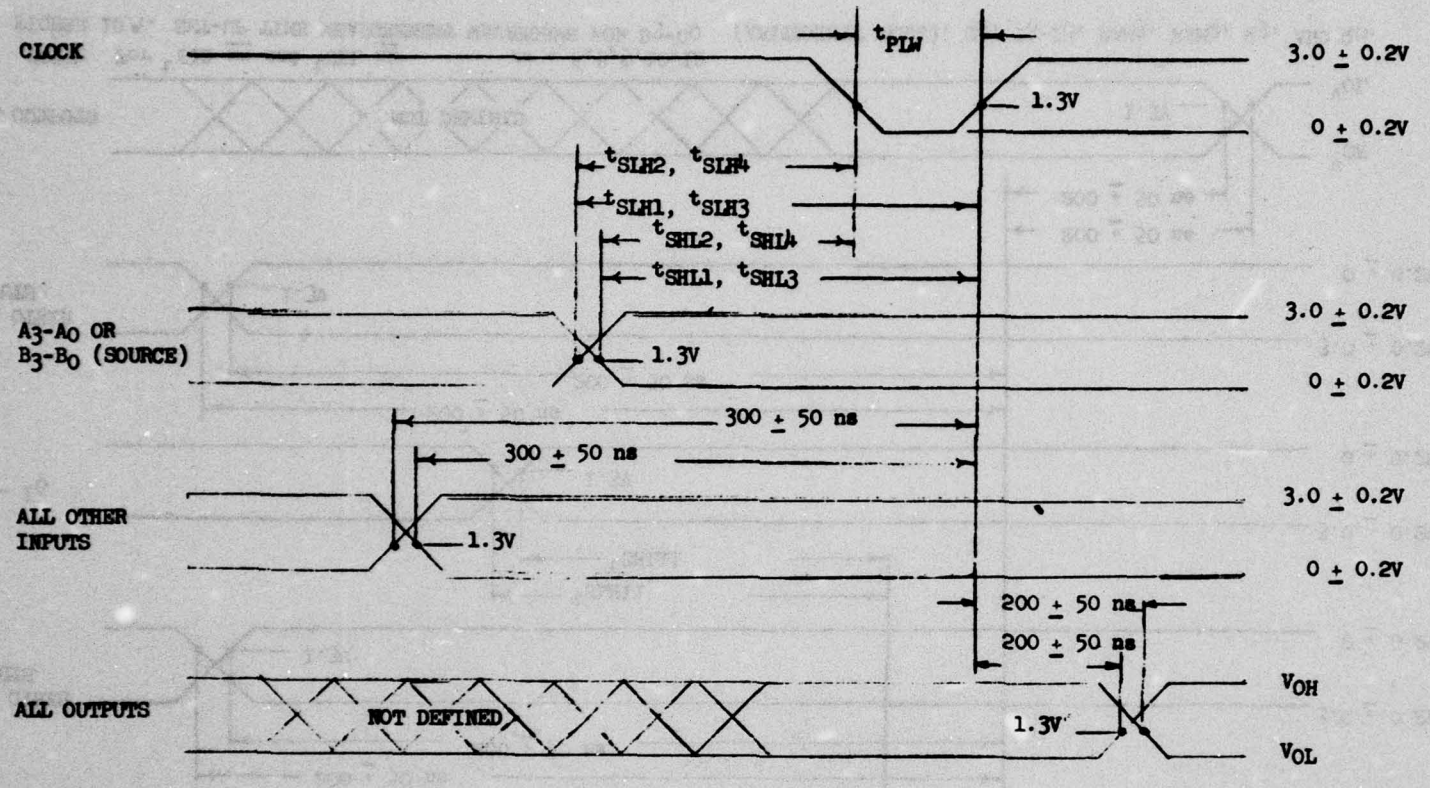
NOTE 1. For t_{PLH} xx, t_{PHL} xx: xx equals 01 through 47. For t_{RHL} y and t_{RLH} y y = 1 through 5.
NOTE 2. Return to input complement pulse width is 200 ns measured at 1.3V.
NOTE 3. The input under test is returned to input complement after the processor is clocked and then back to its true state to ensure that the measured output delay is a function only of the input under test.

FIGURE 7. HOLD TIME AND COMBINATIONAL INPUT TO OUTPUT PROPAGATION DELAY MEASUREMENT WAVEFORMS.



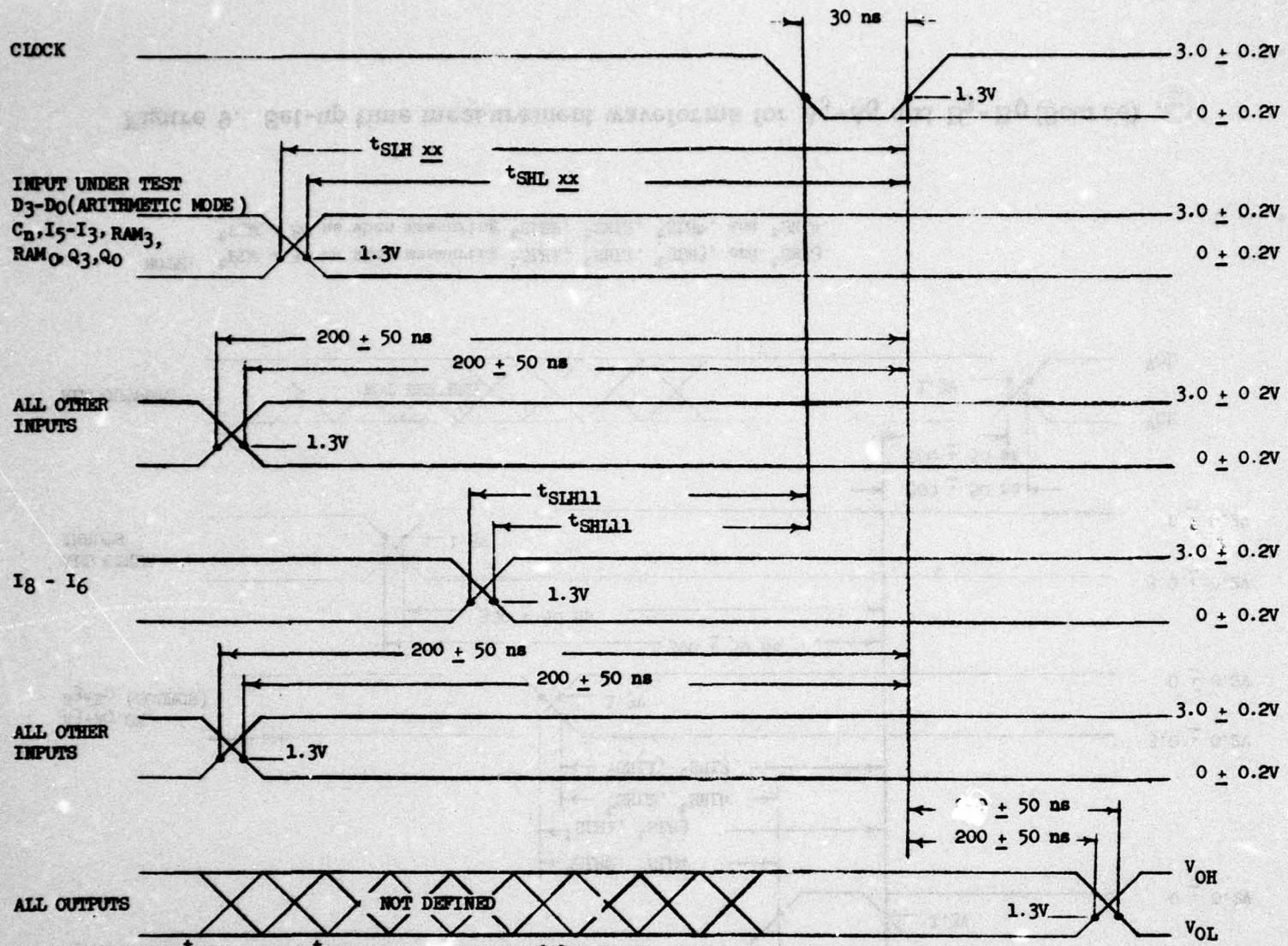
NOTE: For t_{PHL} xx and t_{PLH} xx xx - 48 through 55

FIGURE 8. CLOCK TO OUTPUT PROPAGATION DELAY MEASUREMENT WAVEFORM



NOTE: t_{PLW} = 30 ns when measuring t_{SLH1}, t_{SHL1}, t_{SLH3}, and t_{SHL3}.
t_{PLW} = 80 ns when measuring t_{SLH2}, t_{SHL2}, t_{SLH4}, and t_{SHL4}.

Figure 9. Set-up time measurement waveforms for A_3-A_0 and B_3-B_0 (Source)



NOTE: For t_{SLH} xx and t_{SHL} xx xx = 6,8,9,10.12

FIGURE 10A. SET-UP TIME MEASUREMENT WAVEFORMS FOR D_3-D_0 (ARITHMETIC MODE), C_n, I_8-I_0, RAM_3, RAM_0, Q_3, AND Q_0.

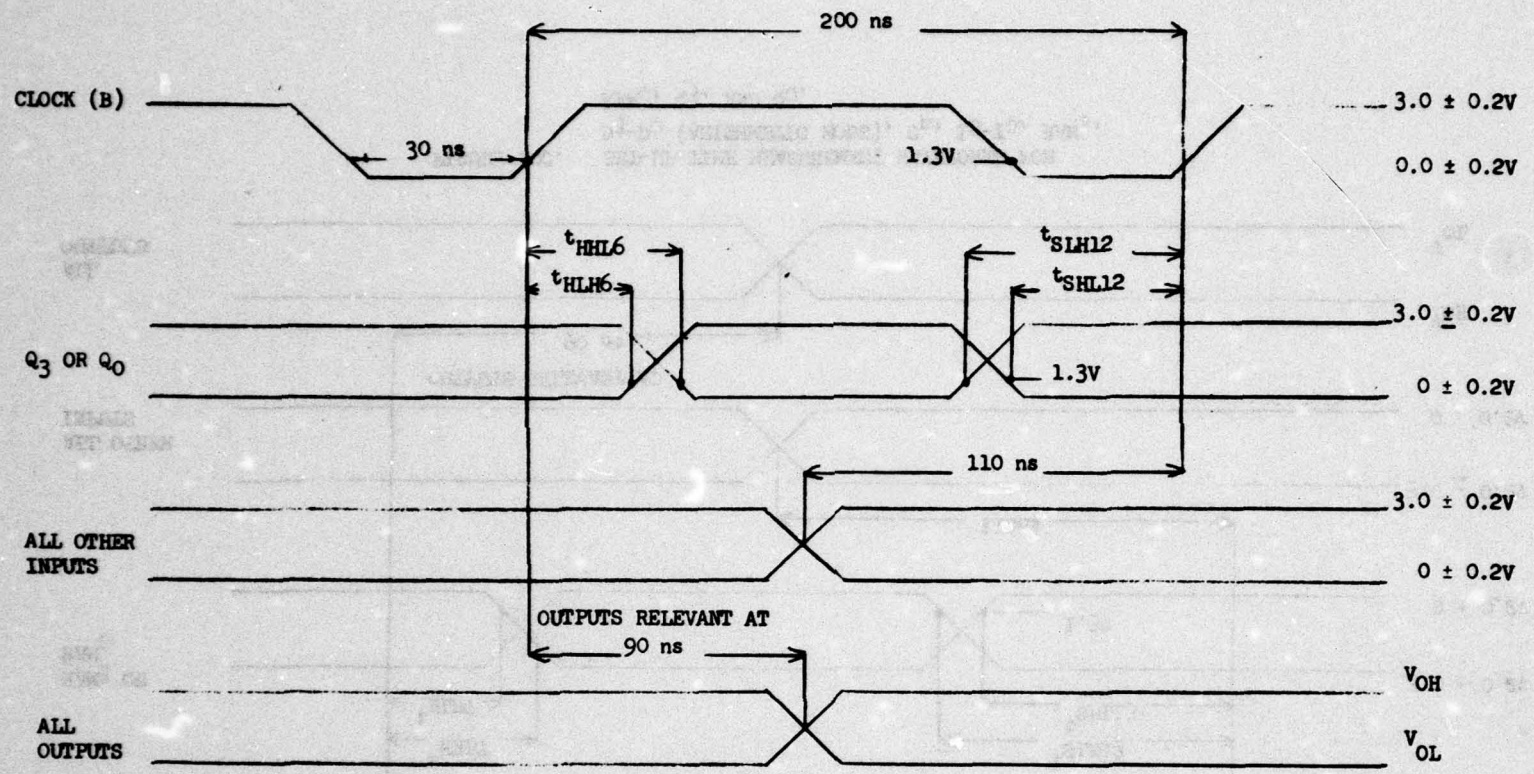


FIGURE 10E. - SET-UP TIME MEASUREMENT WAVEFORMS FOR D_3-D_0 (ARITHMETIC MODE), C_n, I_8-I_0, RAM_3, RAM_0, Q_3, AND Q_0.

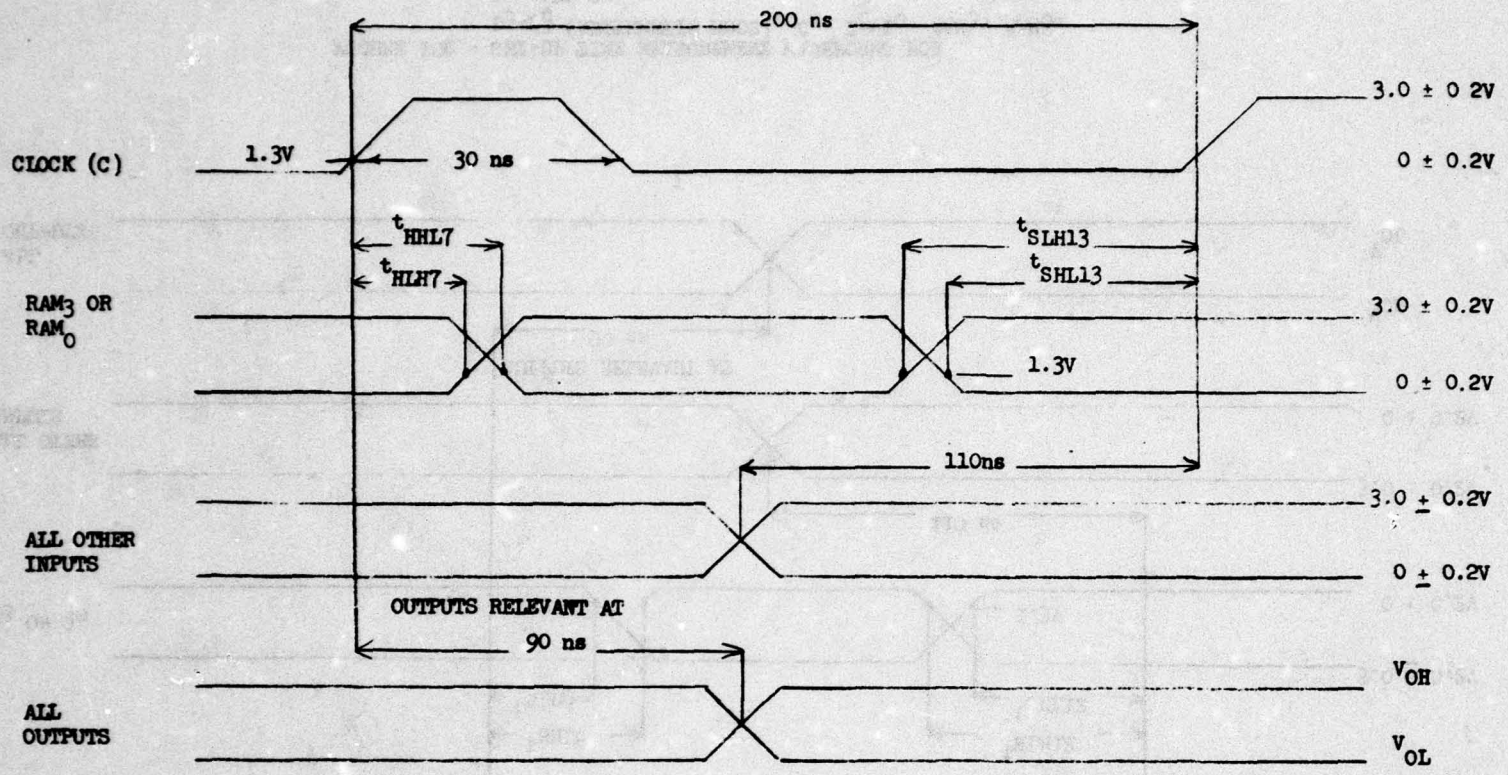


FIGURE 10C. SET-UP TIME MEASUREMENT WAVEFORMS FOR D_3-D_0 (ARITHMETIC MODE), C_n, I_8-I_0, RAM_3, RAM_0, Q_3, AND Q_0.

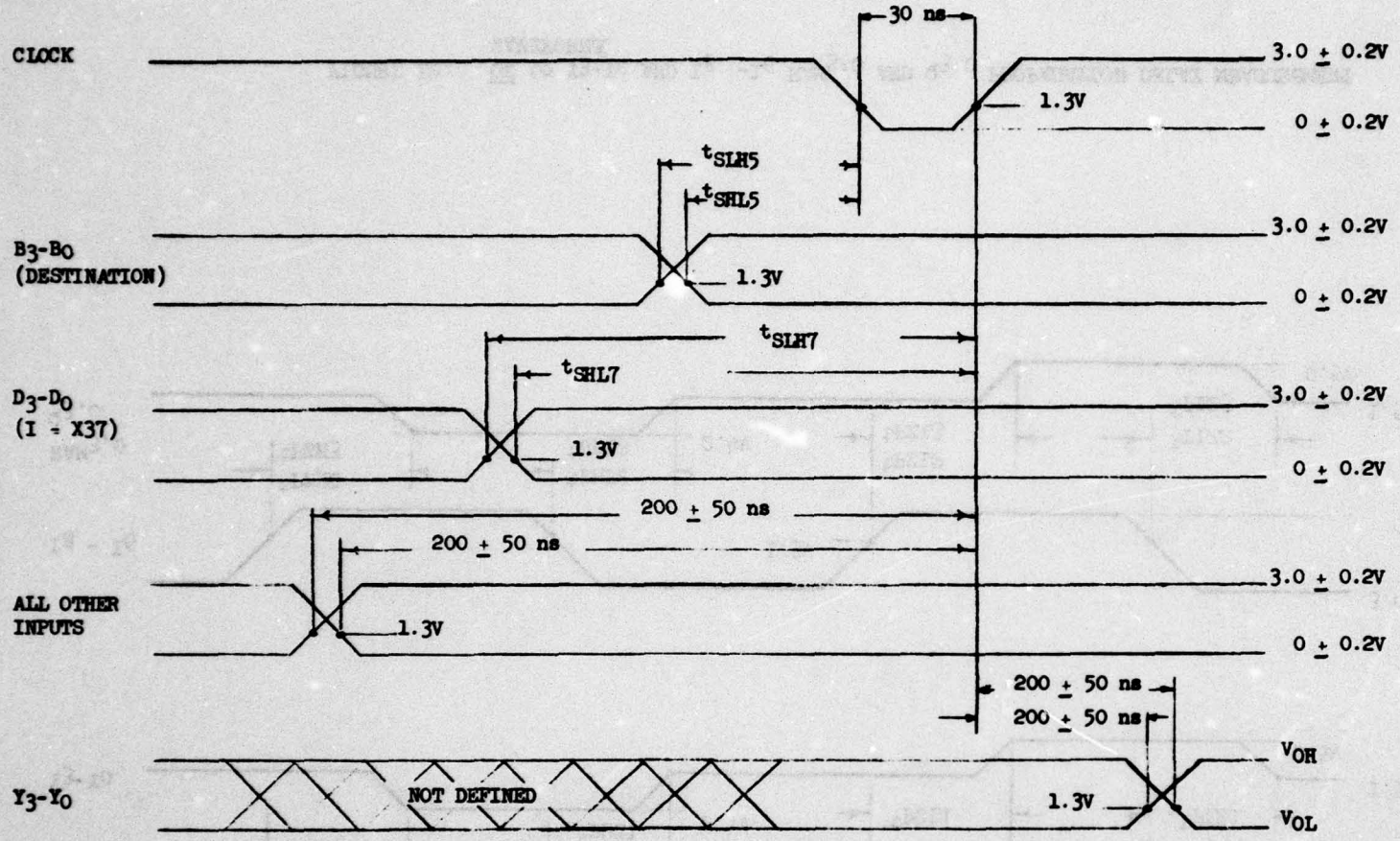


FIGURE 11. SET-UP TIME MEASUREMENT WAVEFORMS FOR B_3-B_0 (DESTINATION) AND D_3-D_0 (I = X37)

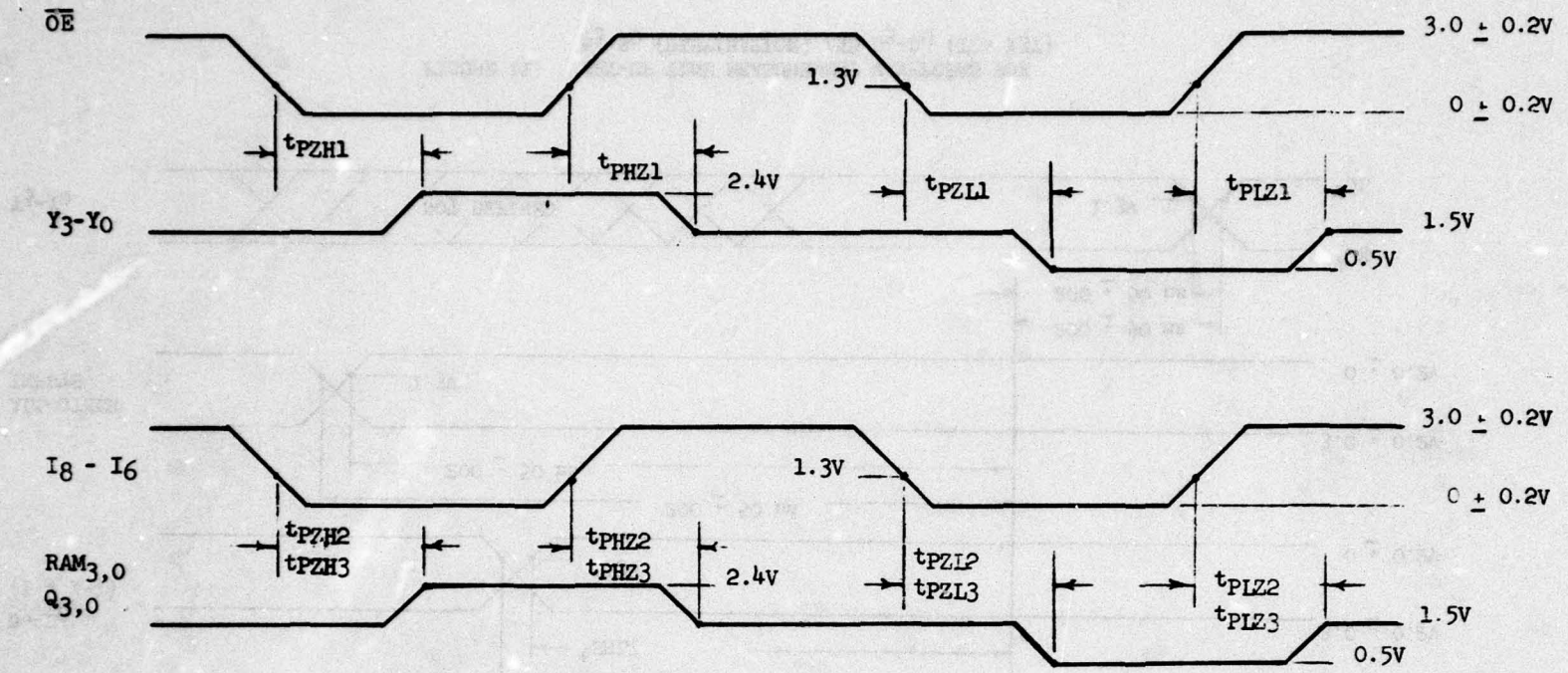
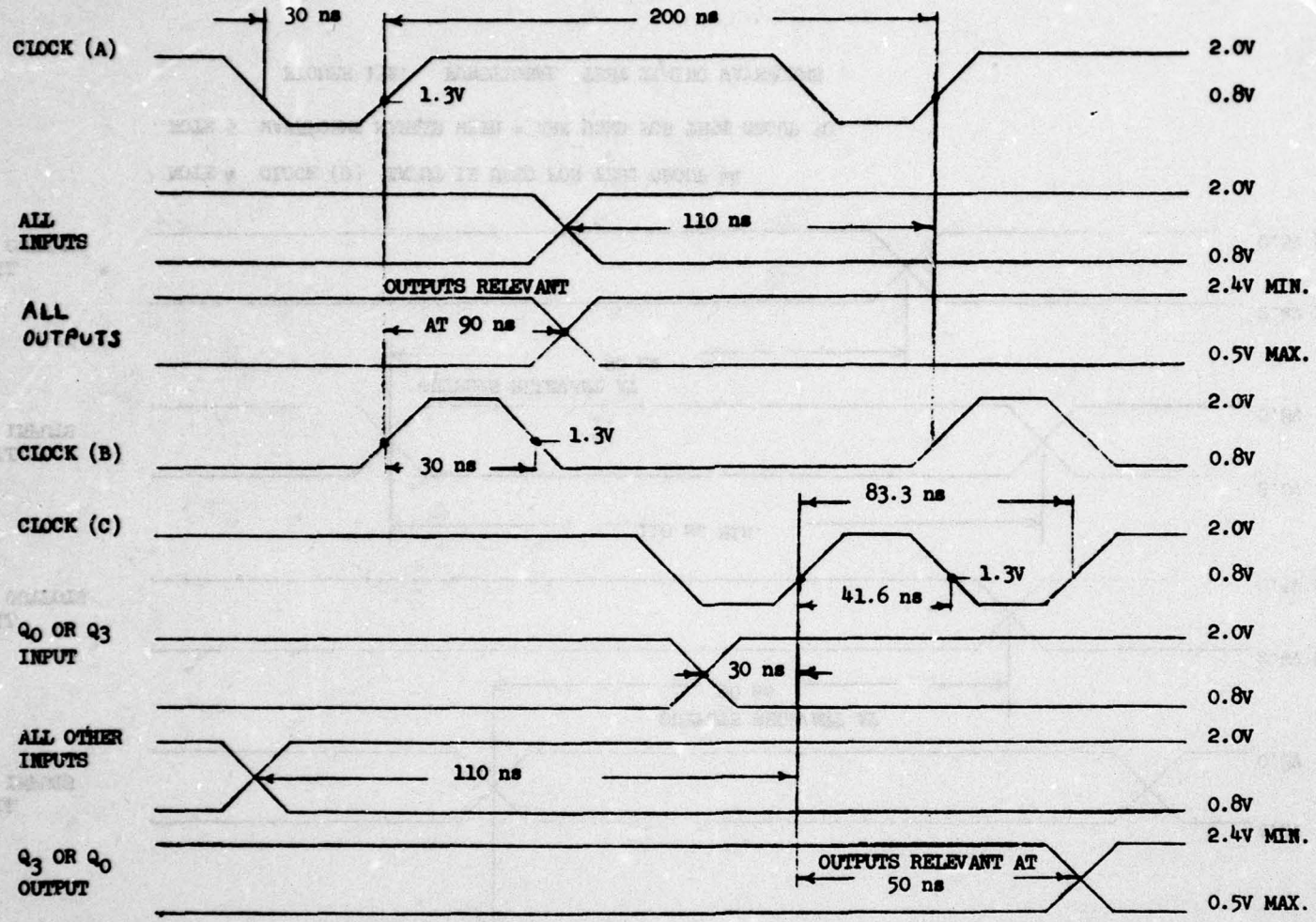


FIGURE 12. $\overline{OE}$ to Y_3-Y_0 AND I_8 -1_6 $RAM_{3,0}$ AND $Q_{3,0}$ PROPAGATION DELAY MEASUREMENT WAVEFORMS.

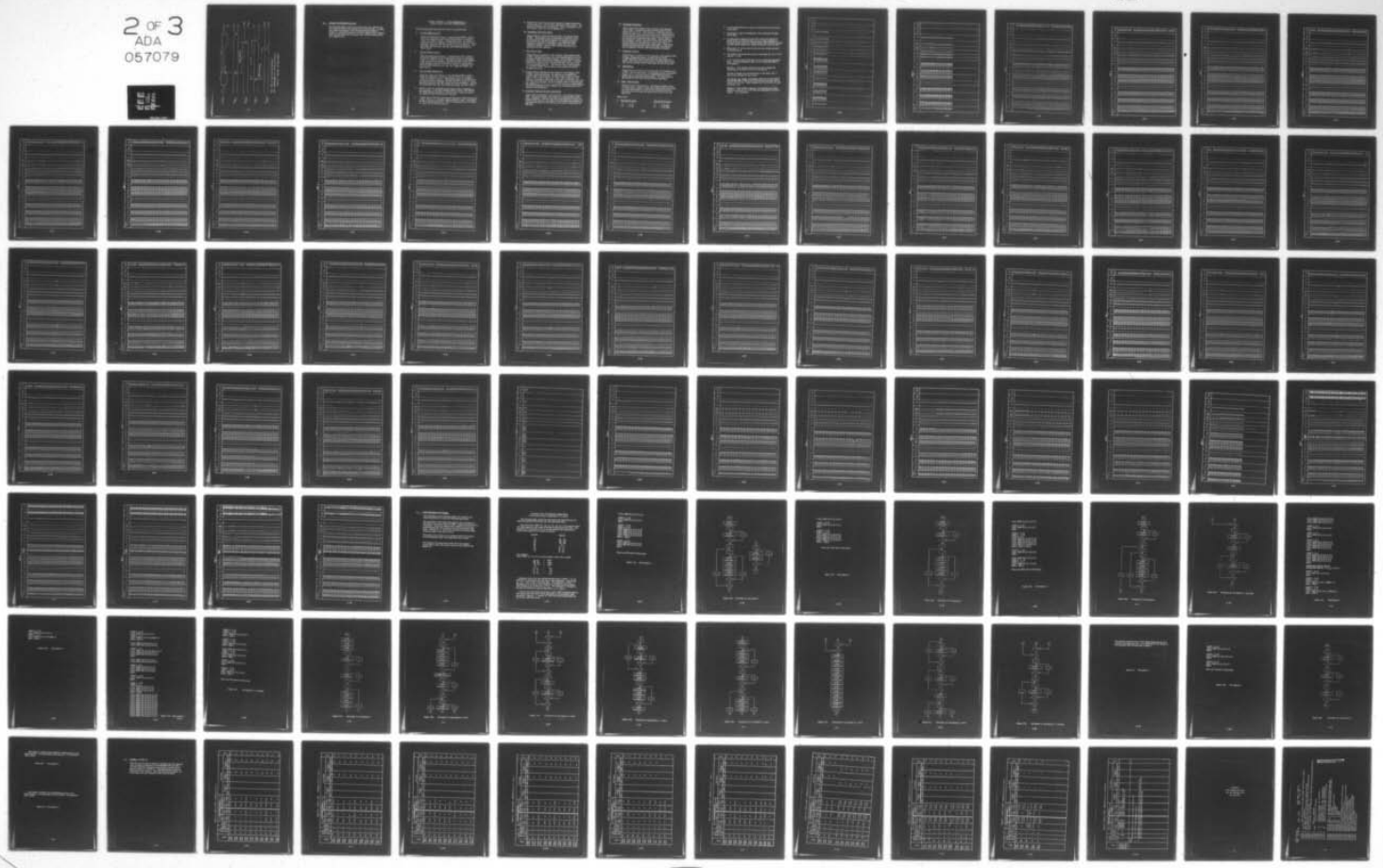


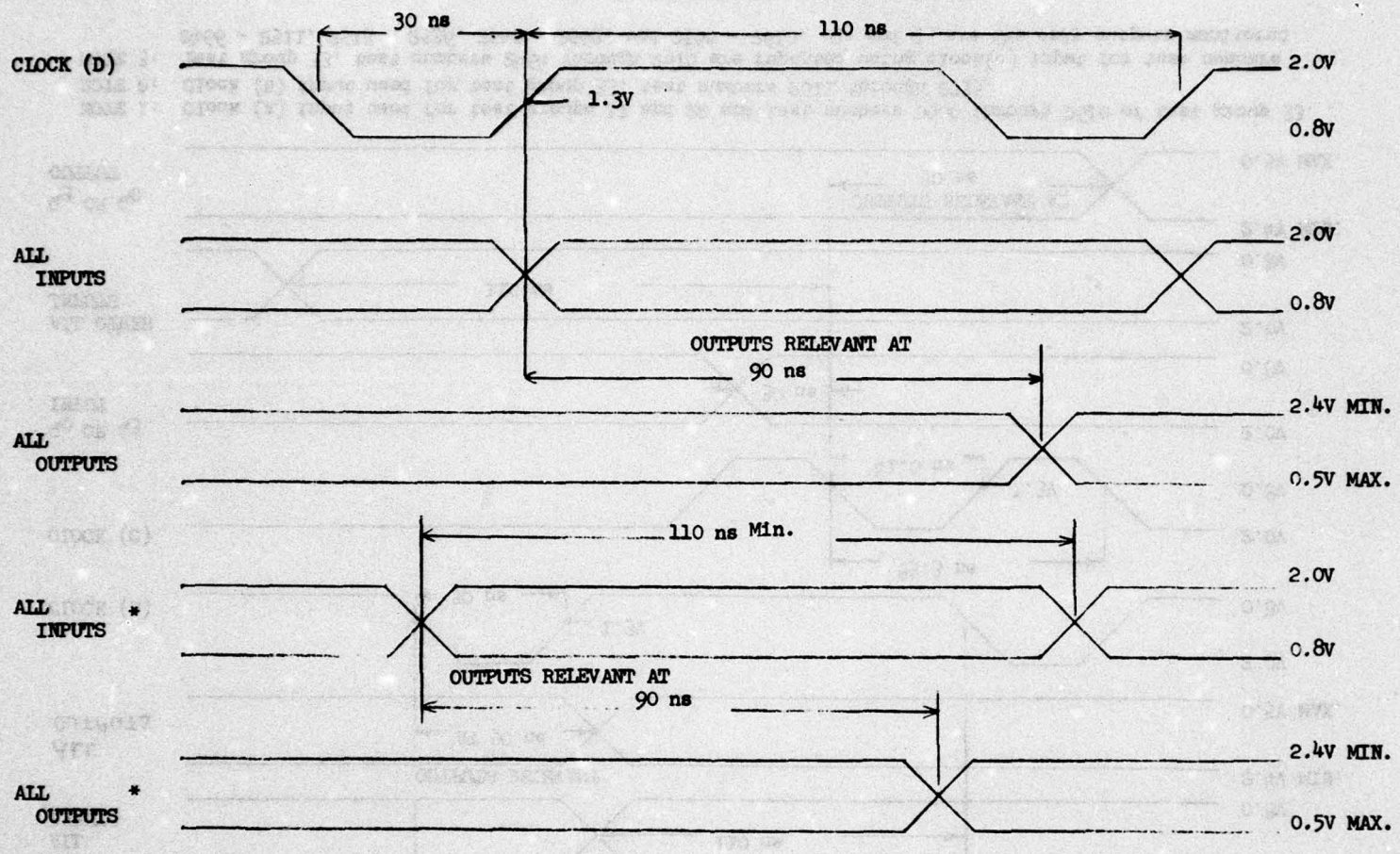
NOTE 1: Clock (A) input used for test groups 11 and 22 and test numbers 0000 through 2610 of test group 33.
NOTE 2: Clock (B) input used for test group 33, test numbers 2611 through 2735.
NOTE 3: Test group 33, test numbers 2464 through 2610 are repeated using clock(c) input for test numbers 2466 - 2511, 2513 - 2536, 2540 - 2563, and 2565 - 2610. Q_3 and Q_0 are the only outputs monitored.

FIGURE 13A. FUNCTIONAL TEST TIMING WAVEFORMS

AD-A057 079 GENERAL ELECTRIC CO PITTSFIELD MASS F/G 9/2
CHARACTERIZATION OF COMPLEX MICROPROCESSORS AND SUPPORT CHIPS.(U)
JUN 78 T M OSTROWSKI F30602-77-C-0012
UNCLASSIFIED RADC-TR-78-138 NL

2 OF 3
ADA
057079





NOTE 4 CLOCK (D) INPUT IS USED FOR TEST GROUP 44

NOTE 5 WAVEFORMS MARKED WITH * ARE USED FOR TEST GROUP 30

FIGURE 13B. FUNCTIONAL TEST TIMING WAVEFORMS

iv. Changes to the Functional Tests

The following pages contain information which was added to the slash sheet to clarify and enchance the functional tests. Included are verbal descriptions of the functional tests provided by Vendor A, verbal descriptions of the tests added by GE, clarified notes for performing the functional tests, and the vectors which were added by GE.

TABLE V GROUP A, TEST SUBGROUPS 7, 8
TABLE NOTES AND TEST DESCRIPTION

The following outline describes the Table V functional tests:

1. A-Port Galpat via ALU

   These are tests (Test Group 11, Test Numbers 0000 to 1015) in which the A-address of the 2-port RAM is tested for Galloping "ones" in a field of "zeros." During these tests, the B-address is the same as the A-address and OP code 337 is used for a write operation, while OP code 134 is used for a read operation. The four shift-operation pins, Q_0, Q3, and RAM_0 and RAM_3 are "don't cares".

2. B-Port Galpat via ALU

   These are tests (Test Group 11, Test Numbers 1016 to 2033) in which the B-address of the 2-port RAM is tested for Galloping "ones" in a field of "zeros." During these tests, the A-address is the inverse of the B-address and OP code 337 is used for a write operation while OP code 133 is used for a read operation. The four shift-operation pins, Q_0, Q_3, RAM_0 and RAM_3, are "don't cares".

3. A-Port Galpat Bypass ALU

   These are tests (Test Group 11, Test Numbers 2034 to 3054) in which the A-address of the 2-port RAM is tested for Galloping "ones" in a field of "zeros." During these tests, the B-address is the inverse of the A-address, and OP code 337 is used for a write operation while OP code 233 is used for a read operation. The four shift-operation pins, Q_0, Q_3, RAM_0 and RAM_3, are "don't cares".

4. Repeat 1 above by inverting the Data and Y output information on D_{3-0} and Y_{3-0} All other outputs are "don't cares." The pattern for these tests is not printed. This performs Galloping "zeros" in a field of "ones" for the A-Port via ALU.

5. Repeat Item 2 above by inverting the Data and Y output information on D_{3-} and Y_{3-0} All other outputs are "don't cares." The pattern for these tests is not printed. This is Galloping "zeros" in a field of "ones" for the B-Port via ALU.

6. Repeat Item 3 above by inverting Data and Y output information on D_{3-0} and Y_{3-0}. All the other outputs are "don't cares". The pattern for these tests is not printed. This is Galloping "zeros" in a field of "ones" for A-Port bypass ALU.

6A. Destination Code and Control

These tests are included in test group 30, test numbers 0000 to 0251. During these tests the destination codes are cycled through and the RAM and Q register are checked to see that they contain the correct information. In addition the high impedance capability of the RAM_3, RAM_0, Q_3, Q_0, and Y outputs is checked. Various other control functions of the processor are also checked.

7. ALU Source Code

These tests are included in Test Group 33, Test Numbers 0000 to 0022. During these tests, the A and B-addresses are at word locations preloaded with known values. The Q register is also preloaded. Then, with the ALU destination OP code = 1 (No OP) and the ALU function code = 6 (exclusive OR), the source code is cycled through from 0-7. The function code is then modified to 7 (exclusive NOR) and the source code sequence is cycled through once more.

8. These tests are included in Test Group 33, Test Numbers 0023 to 0442. During these tests, the memory is preloaded with content equal to the address. In other words, word 0 is loaded with 0, word 1 with 1, and so on. Then, with A-address = B-address, a destination OP code of 1 (No OP), and a source OP code of 1 (A&B Port selected), the ALU function code is cycled through the sequence of 7, 5, 4, 0, 1, 3, 2, 6 for every set of A&B address. This whole sequence is then repeated with A-address equal to the inverse of the B-address.

9. Arithmetic Operation & Carry Generation

These tests are included in Test Group 33, Test Numbers 0443 to 1462. During these tests, the memory is preloaded with content equal to address. With OP code 105, which adds the D input to the A-Port of the memory, the tester cycles through every possible D input added to every word in memory with carry in being both one and zero.

10. Q Register Operation

These tests are included in Test Group 33, Test Numbers 1463 to 2463. During these tests, the Q register is first loaded with all zeros. Then with C_n = 0 and with OP code 006 which loads the Q register with the sum of data input and the Q register contents on every clock cycle, the device is clocked through all possible data inputs. The C_n input is then changed to a ONE, and with OP code 016, which loads the Q register with the difference of Q-D, the device is clocked through all possible data inputs again. This checks both the add and subtract modes of the ALU, the internal-carry-lookahead circuitry and the Q register operation.

11. Q Register Shifting

These tests are included in Test Group 33, Test Numbers 2464 to 2610. During these tests, a unique string of data (11100001010011011110) is shifted into the appropriate shift inputs. OP codes used in this group of tests are 432 for shift left, 532 for no shift, 632 for shift right and 732 for no shift.

12. RAM Shifting

These tests are included in Test Group 33, Test Numbers 2611 to 2735. During these tests, A and B-address are incremented from 0 to 15. A string of data (11100001010011011110) is shifted into the appropriate shift inputs. OP codes used are 434 and 533 for left shift, 634 and 733 for right shift.

13. Read - Modify-Write

These are tests (Test Group 44, Test Numbers 0000 to 0337) in which a read - modify - write test is performed on the RAM. OP codes 324 and 323 are used for the inversion and write operations while OPcodes 134 and 133 are used for the read operations.

Table Notes:

1. FOR INPUT DATA		FOR OUTPUT DATA	
"1"	= 2.0V	"1"	= 2.4V Min.
"0"	= 0.8V	"0"	= 0.5V Max.

2. A test is identified by the values of test group and test number in the table.

3. Any output or input not designated in the functional test table is left open.

4. A clock pulse is applied for each test except Test Group 30. Output levels are checked after the low to high transition of the clock except during the "RAM shifting' tests (33 2611 through 33 2735) where outputs are checked during the clock low time.

5. $\overline{OE}$ is logic "0" for the entire functional test except as stated in Test Group 30.

6. The Table V functional tests shall be replicated for Vcc = 4.5V and Vcc = 5.5V.

7. A "Z' in Test Group 30 indicates a pin is in the high impedance state. The high impedance state can be verified by either of two methods.

   Method 1 - This method consists of forcing a voltage and measuring the current into or out of the device.

   For the Y outputs, the current should be less than ± 50 u a when both 2.4Vand 0.5V are forced.

   For the Q_3, Q_0, RAM_3, and RAM_0 outputs the current should be less than 100 ua when 2.4V is forced and less than -800 ua when 0.5V is forced. Both voltages have to be forced for each occurence of Z.

   Method 2 - This method consists of verifying that the output floats to a level of 1.5 ± 0.5V when the appropriate load from Figure 6 is connected.

SET 1

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
1	0000	0017	0000	1	0001	0071	0000	0	1	0	1	0	1		
2	0000	0017	0000	1	0001	0051	0017	0	0	1	1	1	0		
3	0000	0017	0000	1	0001	0041	0000	0	1	0	1	1	1		
4	0000	0017	0000	1	0001	0001	0000	0	1	0	1	0	1		
5	0000	0017	0000	1	0001	0011	0017	0	0	1	1	0	0		
6	0000	0017	0000	1	0001	0031	0017	0	1	1	1	1	0		
7	0000	0017	0000	1	0001	0021	0001	1	1	0	0	0	0		
8	0000	0017	0000	1	0001	0061	0017	1	1	1	0	0	0		

SET 2

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
1	0012	0000	0001	0	0000	0037	0001	0	0	0	1	1	0		
2	0000	0012	0004	0	0003	0037	0004	0	0	0	1	1	0		
3	0012	0000	0002	0	0003	0037	0002	0	0	0	1	1	0		
4	0012	0000	0010	0	0001	0060	0005	1	0	0	1	0	0		
5	0012	0000	0010	0	0001	0061	0006	1	0	0	1	0	0		
6	0012	0000	0010	0	0001	0062	0001	1	1	0	0	0	0		
7	0012	0000	0010	0	0001	0063	0002	1	1	0	0	0	0		
8	0012	0000	0010	0	0001	0064	0004	1	1	0	0	0	0		
9	0012	0000	0010	0	0001	0065	0014	1	0	1	1	1	0		
10	0012	0000	0010	0	0001	0066	0011	1	0	1	1	1	0		
11	0012	0000	0010	0	0001	0067	0010	0	0	1	1	1	0		
12	0012	0000	0010	0	0001	0070	0012	0	0	1	1	0	0		
13	0012	0000	0010	0	0001	0071	0011	0	0	1	1	0	0		
14	0012	0000	0010	0	0001	0072	0016	0	0	1	1	0	0		
15	0012	0000	0010	0	0001	0073	0015	0	0	1	1	0	0		
16	0012	0000	0010	0	0001	0074	0013	0	0	1	1	0	0		
17	0012	0000	0010	0	0001	0075	0003	0	0	0	1	0	0		
18	0012	0000	0010	0	0001	0076	0006	0	0	0	1	0	0		
19	0012	0000	0010	0	0001	0077	0007	0	0	0	1	0	0		

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{3-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	C30	R30
1	0001	0001	0000	0	0003	0037	0000	0	0	0	1	1	1		
2	0001	0001	0001	0	0004	0034	0000	0	0	0	1	1	1		10
3	0001	0001	0001	0	0004	0034	0010	0	0	1	1	1	0		10
4	0001	0001	0001	0	0004	0034	0014	0	0	1	1	1	0		10
5	0001	0001	0001	0	0004	0034	0016	0	0	1	1	1	0		00
6	0001	0001	0001	0	0004	0034	0007	0	0	0	1	1	0		01
7	0001	0001	0001	0	0004	0034	0003	0	0	0	1	1	0		01
8	0001	0001	0001	0	0004	0034	0001	0	0	0	1	1	0		01
9	0001	0001	0001	0	0004	0034	0000	0	0	0	1	1	1		10
10	0001	0001	0001	0	0004	0034	0010	0	0	1	1	1	0		00
11	0001	0001	0001	0	0004	0034	0004	0	0	0	1	1	0		10
12	0001	0001	0001	0	0004	0034	0012	0	0	1	1	1	0		00
13	0001	0001	0001	0	0004	0034	0005	0	0	0	1	1	0		01
14	0001	0001	0001	0	0004	0034	0002	0	0	0	1	1	0		10
15	0001	0001	0001	0	0004	0034	0011	0	0	1	1	1	0		11
16	0001	0001	0001	0	0004	0034	0014	0	0	1	1	1	0		00
17	0001	0001	0001	0	0004	0034	0006	0	0	0	1	1	0		10
18	0001	0001	0001	0	0004	0034	0013	0	0	1	1	1	0		11
19	0001	0001	0001	0	0004	0034	0015	0	0	1	1	1	0		11
20	0001	0001	0001	0	0004	0034	0016	0	0	1	1	1	0		10
21	0001	0001	0001	0	0004	0034	0017	0	1	1	0	0	0		01
22	0001	0001	0000	0	0003	0037	0000	0	0	0	1	1	1		
23	0001	0001	0001	0	0005	0033	0000	0	0	0	1	1	1		10
24	0001	0001	0001	0	0005	0033	0010	0	0	1	1	1	0		10
25	0001	0001	0001	0	0005	0033	0014	0	0	1	1	1	0		10
26	0001	0001	0001	0	0005	0033	0016	0	0	1	1	1	0		00
27	0001	0001	0001	0	0005	0033	0007	0	0	0	1	1	0		01
28	0001	0001	0001	0	0005	0033	0003	0	0	0	1	1	0		01
29	0001	0001	0001	0	0005	0033	0001	0	0	0	1	1	0		01
30	0001	0001	0001	0	0005	0033	0000	0	0	0	1	1	1		10
31	0001	0001	0001	0	0005	0033	0010	0	0	1	1	1	0		00
32	0001	0001	0001	0	0005	0033	0004	0	0	0	1	1	0		10
33	0001	0001	0001	0	0005	0033	0012	0	0	1	1	1	0		00
34	0001	0001	0001	0	0005	0033	0005	0	0	0	1	1	0		01

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
35	0001	0001	0001	0	0005	0033	0002	0	0	0	1	1	0		10
36	0001	0001	0001	0	0005	0033	0011	0	0	1	1	1	0		11
37	0001	0001	0001	0	0005	0033	0014	0	0	1	1	1	0		00
38	0001	0001	0001	0	0005	0033	0006	0	0	0	1	1	0		10
39	0001	0001	0001	0	0005	0033	0013	0	0	1	1	1	0		11
40	0001	0001	0001	0	0005	0033	0015	0	0	1	1	1	0		11
41	0001	0001	0001	0	0005	0033	0016	0	0	1	1	1	0		10
42	0001	0001	0001	0	0005	0033	0017	0	1	1	0	0	0		01
43	0001	0001	0000	0	0003	0037	0000	0	0	0	1	1	1		
44	0001	0001	0001	0	0006	0034	0000	0	0	0	1	1	1		01
45	0001	0001	0001	0	0006	0034	0001	0	0	0	1	1	0		01
46	0001	0001	0001	0	0006	0034	0003	0	0	0	1	1	0		01
47	0001	0001	0001	0	0006	0034	0007	0	0	0	1	1	0		00
48	0001	0001	0001	0	0006	0034	0016	0	0	1	1	1	0		10
49	0001	0001	0001	0	0006	0034	0014	0	0	1	1	1	0		10
50	0001	0001	0001	0	0006	0034	0010	0	0	1	1	1	0		10
51	0001	0001	0001	0	0006	0034	0000	0	0	0	1	1	1		01
52	0001	0001	0001	0	0006	0034	0001	0	0	0	1	1	0		00
53	0001	0001	0001	0	0006	0034	0002	0	0	0	1	1	0		01
54	0001	0001	0001	0	0006	0034	0005	0	0	0	1	1	0		00
55	0001	0001	0001	0	0006	0034	0012	0	0	1	1	1	0		10
56	0001	0001	0001	0	0006	0034	0004	0	0	0	1	1	0		01
57	0001	0001	0001	0	0006	0034	0011	0	0	1	1	1	0		11
58	0001	0001	0001	0	0006	0034	0003	0	0	0	1	1	0		00
59	0001	0001	0001	0	0006	0034	0006	0	0	0	1	1	0		01
60	0001	0001	0001	0	0006	0034	0015	0	0	1	1	1	0		11
61	0001	0001	0001	0	0006	0034	0013	0	0	1	1	1	0		11
62	0001	0001	0001	0	0006	0034	0007	0	0	0	1	1	0		01
63	0001	0001	0001	0	0006	0034	0017	0	1	1	0	0	0		10
64	0001	0001	0000	0	0003	0037	0000	0	0	0	1	1	1		
65	0001	0001	0001	0	0007	0033	0000	0	0	0	1	1	1		01
66	0001	0001	0001	0	0007	0033	0001	0	0	0	1	1	0		01
67	0001	0001	0001	0	0007	0033	0003	0	0	0	1	1	0		01
68	0001	0001	0001	0	0007	0033	0007	0	0	0	1	1	0		00

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
69	0001	0001	0001	0	0007	0033	0016	0	0	1	1	1	0		10
70	0001	0001	0001	0	0007	0033	0014	0	0	1	1	1	0		10
71	0001	0001	0001	0	0007	0033	0010	0	0	1	1	1	0		10
72	0001	0001	0001	0	0007	0033	0000	0	0	0	1	1	1		01
73	0001	0001	0001	0	0007	0033	0001	0	0	0	1	1	0		00
74	0001	0001	0001	0	0007	0033	0002	0	0	0	1	1	0		01
75	0001	0001	0001	0	0007	0033	0005	0	0	0	1	1	0		00
76	0001	0001	0001	0	0007	0033	0012	0	0	1	1	1	0		10
77	0001	0001	0001	0	0007	0033	0004	0	0	0	1	1	0		01
78	0001	0001	0001	0	0007	0033	0011	0	0	1	1	1	0		11
79	0001	0001	0001	0	0007	0033	0003	0	0	0	1	1	0		00
80	0001	0001	0001	0	0007	0033	0006	0	0	0	1	1	0		01
81	0001	0001	0001	0	0007	0033	0015	0	0	1	1	1	0		11
82	0001	0001	0001	0	0007	0033	0013	0	0	1	1	1	0		11
83	0001	0001	0001	0	0007	0033	0007	0	0	0	1	1	0		01
84	0001	0001	0001	0	0007	0033	0017	0	1	1	0	0	0		10
85	0002	0002	0000	0	0003	0037	0000	0	0	0	1	1	1		
86	0002	0002	0002	0	0004	0034	0000	0	0	0	1	1	1		10
87	0002	0002	0002	0	0004	0034	0010	0	0	1	1	1	0		10
88	0002	0002	0002	0	0004	0034	0014	0	0	1	1	1	0		10
89	0002	0002	0002	0	0004	0034	0016	0	0	1	1	1	0		00
90	0002	0002	0002	0	0004	0034	0007	0	0	0	1	1	0		01
91	0002	0002	0002	0	0004	0034	0003	0	0	0	1	1	0		01
92	0002	0002	0002	0	0004	0034	0001	0	0	0	1	1	0		01
93	0002	0002	0002	0	0004	0034	0000	0	0	0	1	1	1		10
94	0002	0002	0002	0	0004	0034	0010	0	0	1	1	1	0		00
95	0002	0002	0002	0	0004	0034	0004	0	0	0	1	1	0		10
96	0002	0002	0002	0	0004	0034	0012	0	0	1	1	1	0		00
97	0002	0002	0002	0	0004	0034	0005	0	0	0	1	1	0		01
98	0002	0002	0002	0	0004	0034	0002	0	0	0	1	1	0		10
99	0002	0002	0002	0	0004	0034	0011	0	0	1	1	1	0		11
100	0002	0002	0002	0	0004	0034	0014	0	0	1	1	1	0		00
101	0002	0002	0002	0	0004	0034	0006	0	0	0	1	1	0		10
102	0002	0002	0002	0	0004	0034	0013	0	0	1	1	1	0		11

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
103	0002	0002	0002	0	0004	0034	0015	0	0	1	1	1	0		11
104	0002	0002	0002	0	0004	0034	0016	0	0	1	1	1	0		10
105	0002	0002	0002	0	0004	0034	0017	0	1	1	0	0	0		01
106	0002	0002	0000	0	0003	0037	0000	0	0	0	1	1	1		
107	0002	0002	0002	0	0005	0033	0000	0	0	0	1	1	1		10
108	0002	0002	0002	0	0005	0033	0010	0	0	1	1	1	0		10
109	0002	0002	0002	0	0005	0033	0014	0	0	1	1	1	0		10
110	0002	0002	0002	0	0005	0033	0016	0	0	1	1	1	0		00
111	0002	0002	0002	0	0005	0033	0007	0	0	0	1	1	0		01
112	0002	0002	0002	0	0005	0033	0003	0	0	0	1	1	0		01
113	0002	0002	0002	0	0005	0033	0001	0	0	0	1	1	0		01
114	0002	0002	0002	0	0005	0033	0000	0	0	0	1	1	1		10
115	0002	0002	0002	0	0005	0033	0010	0	0	1	1	1	0		00
116	0002	0002	0002	0	0005	0033	0004	0	0	0	1	1	0		10
117	0002	0002	0002	0	0005	0033	0012	0	0	1	1	1	0		00
118	0002	0002	0002	0	0005	0033	0005	0	0	0	1	1	0		01
119	0002	0002	0002	0	0005	0033	0002	0	0	0	1	1	0		10
120	0002	0002	0002	0	0005	0033	0011	0	0	1	1	1	0		11
121	0002	0002	0002	0	0005	0033	0014	0	0	1	1	1	0		00
122	0002	0002	0002	0	0005	0033	0006	0	0	0	1	1	0		10
123	0002	0002	0002	0	0005	0033	0013	0	0	1	1	1	0		11
124	0002	0002	0002	0	0005	0033	0015	0	0	1	1	1	0		11
125	0002	0002	0002	0	0005	0033	0016	0	0	1	1	1	0		10
126	0002	0002	0002	0	0005	0033	0017	0	1	1	0	0	0		01
127	0002	0002	0000	0	0003	0037	0000	0	0	0	1	1	1		
128	0002	0002	0002	0	0006	0034	0000	0	0	0	1	1	1		01
129	0002	0002	0002	0	0006	0034	0001	0	0	0	1	1	0		01
130	0002	0002	0002	0	0006	0034	0003	0	0	0	1	1	0		01
131	0002	0002	0002	0	0006	0034	0007	0	0	0	1	1	0		00
132	0002	0002	0002	0	0006	0034	0016	0	0	1	1	1	0		10
133	0002	0002	0002	0	0006	0034	0014	0	0	1	1	1	0		10
134	0002	0002	0002	0	0006	0034	0010	0	0	1	1	1	0		10
135	0002	0002	0002	0	0006	0034	0000	0	0	0	1	1	1		01
136	0002	0002	0002	0	0006	0034	0001	0	0	0	1	1	0		00

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
137	0002	0002	0002	0	0006	0034	0002	0	0	0	1	1	0		01
138	0002	0002	0002	0	0006	0034	0005	0	0	0	1	1	0		00
139	0002	0002	0002	0	0006	0034	0012	0	0	1	1	1	0		10
140	0002	0002	0002	0	0006	0034	0004	0	0	0	1	1	0		01
141	0002	0002	0002	0	0006	0034	0011	0	0	1	1	1	0		11
142	0002	0002	0002	0	0006	0034	0003	0	0	0	1	1	0		00
143	0002	0002	0002	0	0006	0034	0006	0	0	0	1	1	0		01
144	0002	0002	0002	0	0006	0034	0015	0	0	1	1	1	0		11
145	0002	0002	0002	0	0006	0034	0013	0	0	1	1	1	0		11
146	0002	0002	0002	0	0006	0034	0007	0	0	0	1	1	0		01
147	0002	0002	0002	0	0006	0034	0017	0	1	1	0	0	0		10
148	0002	0002	0000	0	0003	0037	0000	0	0	0	1	1	1		
149	0002	0002	0002	0	0007	0033	0000	0	0	0	1	1	1		01
150	0002	0002	0002	0	0007	0033	0001	0	0	0	1	1	0		01
151	0002	0002	0002	0	0007	0033	0003	0	0	0	1	1	0		01
152	0002	0002	0002	0	0007	0033	0007	0	0	0	1	1	0		00
153	0002	0002	0002	0	0007	0033	0016	0	0	1	1	1	0		10
154	0002	0002	0002	0	0007	0033	0014	0	0	1	1	1	0		10
155	0002	0002	0002	0	0007	0033	0010	0	0	1	1	1	0		10
156	0002	0002	0002	0	0007	0033	0000	0	0	0	1	1	1		01
157	0002	0002	0002	0	0007	0033	0001	0	0	0	1	1	0		00
158	0002	0002	0002	0	0007	0033	0002	0	0	0	1	1	0		01
159	0002	0002	0002	0	0007	0033	0005	0	0	0	1	1	0		00
160	0002	0002	0002	0	0007	0033	0012	0	0	1	1	1	0		10
161	0002	0002	0002	0	0007	0033	0004	0	0	0	1	1	0		01
162	0002	0002	0002	0	0007	0033	0011	0	0	1	1	1	0		11
163	0002	0002	0002	0	0007	0033	0003	0	0	0	1	1	0		00
164	0002	0002	0002	0	0007	0033	0006	0	0	0	1	1	0		01
165	0002	0002	0002	0	0007	0033	0015	0	0	1	1	1	0		11
166	0002	0002	0002	0	0007	0033	0013	0	0	1	1	1	0		11
167	0002	0002	0002	0	0007	0033	0007	0	0	0	1	1	0		01
168	0002	0002	0002	0	0007	0033	0017	0	1	1	0	0	0		10
169	0003	0003	0000	0	0003	0037	0000	0	0	0	1	1	1		
170	0003	0003	0003	0	0004	0034	0000	0	0	0	1	1	1		10

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	C_{N4}	OVR	F_0	Q_{30}	R_{30}
171	0003	0003	0003	0	0004	0034	0010	0	0	1	1	1	0		10
172	0003	0003	0003	0	0004	0034	0014	0	0	1	1	1	0		10
173	0003	0003	0003	0	0004	0034	0016	0	0	1	1	1	0		00
174	0003	0003	0003	0	0004	0034	0007	0	0	0	1	1	0		01
175	0003	0003	0003	0	0004	0034	0003	0	0	0	1	1	0		01
176	0003	0003	0003	0	0004	0034	0001	0	0	0	1	1	0		01
177	0003	0003	0003	0	0004	0034	0000	0	0	0	1	1	1		10
178	0003	0003	0003	0	0004	0034	0010	0	0	1	1	1	0		00
179	0003	0003	0003	0	0004	0034	0004	0	0	0	1	1	0		10
180	0003	0003	0003	0	0004	0034	0012	0	0	1	1	1	0		00
181	0003	0003	0003	0	0004	0034	0005	0	0	0	1	1	0		01
182	0003	0003	0003	0	0004	0034	0002	0	0	0	1	1	0		10
183	0003	0003	0003	0	0004	0034	0011	0	0	1	1	1	0		11
184	0003	0003	0003	0	0004	0034	0014	0	0	1	1	1	0		00
185	0003	0003	0003	0	0004	0034	0006	0	0	0	1	1	0		10
186	0003	0003	0003	0	0004	0034	0013	0	0	1	1	1	0		11
187	0003	0003	0003	0	0004	0034	0015	0	0	1	1	1	0		11
188	0003	0003	0003	0	0004	0034	0016	0	0	1	1	1	0		10
189	0003	0003	0003	0	0004	0034	0017	0	1	1	0	0	0		01 ←
190	0003	0003	0000	0	0003	0037	0000	0	0	0	1	1	1		
191	0003	0003	0003	0	0005	0033	0000	0	0	0	1	1	1		10
192	0003	0003	0003	0	0005	0033	0010	0	0	1	1	1	0		10
193	0003	0003	0003	0	0005	0033	0014	0	0	1	1	1	0		10
194	0003	0003	0003	0	0005	0033	0016	0	0	1	1	1	0		00
195	0003	0003	0003	0	0005	0033	0007	0	0	0	1	1	0		01
196	0003	0003	0003	0	0005	0033	0003	0	0	0	1	1	0		01
197	0003	0003	0003	0	0005	0033	0001	0	0	0	1	1	0		01
198	0003	0003	0003	0	0005	0033	0000	0	0	0	1	1	1		10
199	0003	0003	0003	0	0005	0033	0010	0	0	1	1	1	0		00
200	0003	0003	0003	0	0005	0033	0004	0	0	0	1	1	0		10
201	0003	0003	0003	0	0005	0033	0012	0	0	1	1	1	0		00
202	0003	0003	0003	0	0005	0033	0005	0	0	0	1	1	0		01
203	0003	0003	0003	0	0005	0033	0002	0	0	0	1	1	0		10
204	0003	0003	0003	0	0005	0033	0011	0	0	1	1	1	0		11

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	C_{N+4}	OVR	F_0	Q_{30}	R_{30}
205	0003	0003	0003	0	0005	0033	0014	0	0	1	1	1	0		00
206	0003	0003	0003	0	0005	0033	0006	0	0	0	1	1	0		10
207	0003	0003	0003	0	0005	0033	0013	0	0	1	1	1	0		11
208	0003	0003	0003	0	0005	0033	0015	0	0	1	1	1	0		11
209	0003	0003	0003	0	0005	0033	0016	0	0	1	1	1	0		10
210	0003	0003	0003	0	0005	0033	0017	0	1	1	0	0	0		01
211	0003	0003	0000	0	0003	0037	0000	0	0	0	1	1	1		
212	0003	0003	0003	0	0006	0034	0000	0	0	0	1	1	1		01
213	0003	0003	0003	0	0006	0034	0001	0	0	0	1	1	0		01
214	0003	0003	0003	0	0006	0034	0003	0	0	0	1	1	0		01
215	0003	0003	0003	0	0006	0034	0007	0	0	0	1	1	0		00
216	0003	0003	0003	0	0006	0034	0016	0	0	1	1	1	0		10
217	0003	0003	0003	0	0006	0034	0014	0	0	1	1	1	0		10
218	0003	0003	0003	0	0006	0034	0010	0	0	1	1	1	0		10
219	0003	0003	0003	0	0006	0034	0000	0	0	0	1	1	1		01
220	0003	0003	0003	0	0006	0034	0001	0	0	0	1	1	0		00
221	0003	0003	0003	0	0006	0034	0002	0	0	0	1	1	0		01
222	0003	0003	0003	0	0006	0034	0005	0	0	0	1	1	0		00
223	0003	0003	0003	0	0006	0034	0012	0	0	1	1	1	0		10
224	0003	0003	0003	0	0006	0034	0004	0	0	0	1	1	0		01
225	0003	0003	0003	0	0006	0034	0011	0	0	1	1	1	0		11
226	0003	0003	0003	0	0006	0034	0003	0	0	0	1	1	0		00
227	0003	0003	0003	0	0006	0034	0006	0	0	0	1	1	0		01
228	0003	0003	0003	0	0006	0034	0015	0	0	1	1	1	0		11
229	0003	0003	0003	0	0006	0034	0013	0	0	1	1	1	0		11
230	0003	0003	0003	0	0006	0034	0007	0	0	0	1	1	0		01
231	0003	0003	0003	0	0006	0034	0017	0	1	1	0	0	0		10
232	0003	0003	0000	0	0003	0037	0000	0	0	0	1	1	1		
233	0003	0003	0003	0	0007	0033	0000	0	0	0	1	1	1		01
234	0003	0003	0003	0	0007	0033	0001	0	0	0	1	1	0		01
235	0003	0003	0003	0	0007	0033	0003	0	0	0	1	1	0		01
236	0003	0003	0003	0	0007	0033	0007	0	0	0	1	1	0		00
237	0003	0003	0003	0	0007	0033	0016	0	0	1	1	1	0		10
238	0003	0003	0003	0	0007	0033	0014	0	0	1	1	1	0		10

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
239	0003	0003	0003	0	0007	0033	0010	0	0	1	1	1	0		10
240	0003	0003	0003	0	0007	0033	0000	0	0	0	1	1	1		01
241	0003	0003	0003	0	0007	0033	0001	0	0	0	1	1	0		00
242	0003	0003	0003	0	0007	0033	0002	0	0	0	1	1	0		01
243	0003	0003	0003	0	0007	0033	0005	0	0	0	1	1	0		00
244	0003	0003	0003	0	0007	0033	0012	0	0	1	1	1	0		10
245	0003	0003	0003	0	0007	0033	0004	0	0	0	1	1	0		01
246	0003	0003	0003	0	0007	0033	0011	0	0	1	1	1	0		11
247	0003	0003	0003	0	0007	0033	0003	0	0	0	1	1	0		00
248	0003	0003	0003	0	0007	0033	0006	0	0	0	1	1	0		01
249	0003	0003	0003	0	0007	0033	0015	0	0	1	1	1	0		11
250	0003	0003	0003	0	0007	0033	0013	0	0	1	1	1	0		11
251	0003	0003	0003	0	0007	0033	0007	0	0	0	1	1	0		01
252	0003	0003	0003	0	0007	0033	0017	0	1	1	0	0	0		10
253	0004	0004	0000	0	0003	0037	0000	0	0	0	1	1	1		
254	0004	0004	0004	0	0004	0034	0000	0	0	0	1	1	1		10
255	0004	0004	0004	0	0004	0034	0010	0	0	1	1	1	0		10
256	0004	0004	0004	0	0004	0034	0014	0	0	1	1	1	0		10
257	0004	0004	0004	0	0004	0034	0016	0	0	1	1	1	0		00
258	0004	0004	0004	0	0004	0034	0007	0	0	0	1	1	0		01
259	0004	0004	0004	0	0004	0034	0003	0	0	0	1	1	0		01
260	0004	0004	0004	0	0004	0034	0001	0	0	0	1	1	0		01
261	0004	0004	0004	0	0004	0034	0000	0	0	0	1	1	1		10
262	0004	0004	0004	0	0004	0034	0010	0	0	1	1	1	0		00
263	0004	0004	0004	0	0004	0034	0004	0	0	0	1	1	0		10
264	0004	0004	0004	0	0004	0034	0012	0	0	1	1	1	0		00
265	0004	0004	0004	0	0004	0034	0005	0	0	0	1	1	0		01
266	0004	0004	0004	0	0004	0034	0002	0	0	0	1	1	0		10
267	0004	0004	0004	0	0004	0034	0011	0	0	1	1	1	0		11
268	0004	0004	0004	0	0004	0034	0014	0	0	1	1	1	0		00
269	0004	0004	0004	0	0004	0034	0006	0	0	0	1	1	0		10
270	0004	0004	0004	0	0004	0034	0013	0	0	1	1	1	0		11
271	0004	0004	0004	0	0004	0034	0015	0	0	1	1	1	0		11
272	0004	0004	0004	0	0004	0034	0016	0	0	1	1	1	0		10

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
273	0004	0004	0004	0	0004	003 4	00 17	0	1	1	0	0	0		01
274	0004	0004	0000	0	0003	003 7	00 00	0	0	0	1	1	1		
275	0004	0004	0004	0	0005	003 3	00 00	0	0	0	1	1	1		10
276	0004	0004	0004	0	0005	003 3	00 10	0	0	1	1	1	0		10
277	0004	0004	0004	0	0005	003 3	00 14	0	0	1	1	1	0		10
278	0004	0004	0004	0	0005	003 3	00 16	0	0	1	1	1	0		00
279	0004	0004	0004	0	0005	003 3	00 07	0	0	0	1	1	0		01
280	0004	0004	0004	0	0005	003 3	00 03	0	0	0	1	1	0		01
281	0004	0004	0004	0	0005	003 3	00 01	0	0	0	1	1	0		01
282	0004	0004	0004	0	0005	003 3	00 00	0	0	0	1	1	1		10
283	0004	0004	0004	0	0005	003 3	00 10	0	0	1	1	1	0		00
284	0004	0004	0004	0	0005	003 3	00 04	0	0	0	1	1	0		10
285	0004	0004	0004	0	0005	003 3	00 12	0	0	1	1	1	0		00
286	0004	0004	0004	0	0005	003 3	00 05	0	0	0	1	1	0		01
287	0004	0004	0004	0	0005	003 3	00 02	0	0	0	1	1	0		10
288	0004	0004	0004	0	0005	003 3	00 11	0	0	1	1	1	0		11
289	0004	0004	0004	0	0005	003 3	00 14	0	0	1	1	1	0		00
290	0004	0004	0004	0	0005	003 3	00 06	0	0	0	1	1	0		10
291	0004	0004	0004	0	0005	003 3	00 13	0	0	1	1	1	0		11
292	0004	0004	0004	0	0005	003 3	00 15	0	0	1	1	1	0		11
293	0004	0004	0004	0	0005	003 3	00 16	0	0	1	1	1	0		10
294	0004	0004	0004	0	0005	003 3	00 17	0	1	1	0	0	0		01
295	0004	0004	0000	0	0003	003 7	00 00	0	0	0	1	1	1		
296	0004	0004	0004	0	0006	003 4	00 00	0	0	0	1	1	1		01
297	0004	0004	0004	0	0006	003 4	00 01	0	0	0	1	1	0		01
298	0004	0004	0004	0	0006	003 4	00 03	0	0	0	1	1	0		01
299	0004	0004	0004	0	0006	003 4	00 07	0	0	0	1	1	0		00
300	0004	0004	0004	0	0006	003 4	00 16	0	0	1	1	1	0		10
301	0004	0004	0004	0	0006	003 4	00 14	0	0	1	1	1	0		10
302	0004	0004	0004	0	0006	003 4	00 10	0	0	1	1	1	0		10
303	0004	0004	0004	0	0006	003 4	00 00	0	0	0	1	1	1		01
304	0004	0004	0004	0	0006	003 4	00 01	0	0	0	1	1	0		00
305	0004	0004	0004	0	0006	003 4	00 02	0	0	0	1	1	0		01
306	0004	0004	0004	0	0006	003 4	00 05	0	0	0	1	1	0		00

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
307	0004	0004	0004	0	0006	0034	0012	0	0	1	1	1	0		10
308	0004	0004	0004	0	0006	0034	0004	0	0	0	1	1	0		01
309	0004	0004	0004	0	0006	0034	0011	0	0	1	1	1	0		11
310	0004	0004	0004	0	0006	0034	0003	0	0	0	1	1	0		00
311	0004	0004	0004	0	0006	0034	0006	0	0	0	1	1	0		01
312	0004	0004	0004	0	0006	0034	0015	0	0	1	1	1	0		11
313	0004	0004	0004	0	0006	0034	0013	0	0	1	1	1	0		11
314	0004	0004	0004	0	0006	0034	0007	0	0	0	1	1	0		01
315	0004	0004	0004	0	0006	0034	0017	0	1	1	0	0	0		10
316	0004	0004	0000	0	0003	0037	0000	0	0	0	1	1	1		
317	0004	0004	0004	0	0007	0033	0000	0	0	0	1	1	1		01
318	0004	0004	0004	0	0007	0033	0001	0	0	0	1	1	0		01
319	0004	0004	0004	0	0007	0033	0003	0	0	0	1	1	0		01
320	0004	0004	0004	0	0007	0033	0007	0	0	0	1	1	0		00
321	0004	0004	0004	0	0007	0033	0016	0	0	1	1	1	0		10
322	0004	0004	0004	0	0007	0033	0014	0	0	1	1	1	0		10
323	0004	0004	0004	0	0007	0033	0010	0	0	1	1	1	0		10
324	0004	0004	0004	0	0007	0033	0000	0	0	0	1	1	1		01
325	0004	0004	0004	0	0007	0033	0001	0	0	0	1	1	0		00
326	0004	0004	0004	0	0007	0033	0002	0	0	0	1	1	0		01
327	0004	0004	0004	0	0007	0033	0005	0	0	0	1	1	0		00
328	0004	0004	0004	0	0007	0033	0012	0	0	1	1	1	0		10
329	0004	0004	0004	0	0007	0033	0004	0	0	0	1	1	0		01
330	0004	0004	0004	0	0007	0033	0011	0	0	1	1	1	0		11
331	0004	0004	0004	0	0007	0033	0003	0	0	0	1	1	0		00
332	0004	0004	0004	0	0007	0033	0006	0	0	0	1	1	0		01
333	0004	0004	0004	0	0007	0033	0015	0	0	1	1	1	0		11
334	0004	0004	0004	0	0007	0033	0013	0	0	1	1	1	0		11
335	0004	0004	0004	0	0007	0033	0007	0	0	0	1	1	0		01
336	0004	0004	0004	0	0007	0033	0017	0	1	1	0	0	0		10
337	0005	0005	0000	0	0003	0037	0000	0	0	0	1	1	1		
338	0005	0005	0005	0	0004	0034	0000	0	0	0	1	1	1		1
339	0005	0005	0005	0	0004	0034	0010	0	0	1	1	1	0		10
340	0005	0005	0005	0	0004	0034	0014	0	0	1	1	1	0		10

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
341	0005	0005	0005	0	0004	0034	0016	0	0	1	1	1	0		00
342	0005	0005	0005	0	0004	0034	0007	0	0	0	1	1	0		01
343	0005	0005	0005	0	0004	0034	0003	0	0	0	1	1	0		01
344	0005	0005	0005	0	0004	0034	0001	0	0	0	1	1	0		01
345	0005	0005	0005	0	0004	0034	0000	0	0	0	1	1	1		10
346	0005	0005	0005	0	0004	0034	0010	0	0	1	1	1	0		00
347	0005	0005	0005	0	0004	0034	0004	0	0	0	1	1	0		10
348	0005	0005	0005	0	0004	0034	0012	0	0	1	1	1	0		00
349	0005	0005	0005	0	0004	0034	0005	0	0	0	1	1	0		01
350	0005	0005	0005	0	0004	0034	0002	0	0	0	1	1	0		10
351	0005	0005	0005	0	0004	0034	0011	0	0	1	1	1	0		11
352	0005	0005	0005	0	0004	0034	0014	0	0	1	1	1	0		00
353	0005	0005	0005	0	0004	0034	0006	0	0	0	1	1	0		10
354	0005	0005	0005	0	0004	0034	0013	0	0	1	1	1	0		11
355	0005	0005	0005	0	0004	0034	0015	0	0	1	1	1	0		11
356	0005	0005	0005	0	0004	0034	0016	0	0	1	1	1	0		10
357	0005	0005	0005	0	0004	0034	0017	0	1	1	0	0	0		01
358	0005	0005	0000	0	0003	0037	0000	0	0	0	1	1	1		
359	0005	0005	0005	0	0005	0033	0000	0	0	0	1	1	1		10
360	0005	0005	0005	0	0005	0033	0010	0	0	1	1	1	0		10
361	0005	0005	0005	0	0005	0033	0014	0	0	1	1	1	0		10
362	0005	0005	0005	0	0005	0033	0016	0	0	1	1	1	0		00
363	0005	0005	0005	0	0005	0033	0007	0	0	0	1	1	0		01
364	0005	0005	0005	0	0005	0033	0003	0	0	0	1	1	0		01
365	0005	0005	0005	0	0005	0033	0001	0	0	0	1	1	0		01
366	0005	0005	0005	0	0005	0033	0000	0	0	0	1	1	1		10
367	0005	0005	0005	0	0005	0033	0010	0	0	1	1	1	0		00
368	0005	0005	0005	0	0005	0033	0004	0	0	0	1	1	0		10
369	0005	0005	0005	0	0005	0033	0012	0	0	1	1	1	0		00
370	0005	0005	0005	0	0005	0033	0005	0	0	0	1	1	0		01
371	0005	0005	0005	0	0005	0033	0002	0	0	0	1	1	0		10
372	0005	0005	0005	0	0005	0033	0011	0	0	1	1	1	0		11
373	0005	0005	0005	0	0005	0033	0014	0	0	1	1	1	0		00
374	0005	0005	0005	0	0005	0033	0006	0	0	0	1	1	0		10

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CNH	OVR	F_0	Q_{30}	R_{30}
375	0005	0005	0005	0	0005	0033	0013	0	0	1	1	1	0		11
376	0005	0005	0005	0	0005	0033	0015	0	0	1	1	1	0		11
377	0005	0005	0005	0	0005	0033	0016	0	0	1	1	1	0		10
378	0005	0005	0005	0	0005	0033	0017	0	1	1	0	0	0		01
379	0005	0005	0000	0	0003	0037	0000	0	0	0	1	1	1		
380	0005	0005	0005	0	0006	0034	0000	0	0	0	1	1	1		01
381	0005	0005	0005	0	0006	0034	0001	0	0	0	1	1	0		01
382	0005	0005	0005	0	0006	0034	0003	0	0	0	1	1	0		01
383	0005	0005	0005	0	0006	0034	0007	0	0	0	1	1	0		00
384	0005	0005	0005	0	0006	0034	0016	0	0	1	1	1	0		10
385	0005	0005	0005	0	0006	0034	0014	0	0	1	1	1	0		10
386	0005	0005	0005	0	0006	0034	0010	0	0	1	1	1	0		10
387	0005	0005	0005	0	0006	0034	0000	0	0	0	1	1	1		01
388	0005	0005	0005	0	0006	0034	0001	0	0	0	1	1	0		00
389	0005	0005	0005	0	0006	0034	0002	0	0	0	1	1	0		01
390	0005	0005	0005	0	0006	0034	0005	0	0	0	1	1	0		00
391	0005	0005	0005	0	0006	0034	0012	0	0	1	1	1	0		10
392	0005	0005	0005	0	0006	0034	0004	0	0	0	1	1	0		01
393	0005	0005	0005	0	0006	0034	0011	0	0	1	1	1	0		11
394	0005	0005	0005	0	0006	0034	0003	0	0	0	1	1	0		00
395	0005	0005	0005	0	0006	0034	0006	0	0	0	1	1	0		01
396	0005	0005	0005	0	0006	0034	0015	0	0	1	1	1	0		11
397	0005	0005	0005	0	0006	0034	0013	0	0	1	1	1	0		11
398	0005	0005	0005	0	0006	0034	0007	0	0	0	1	1	0		01
399	0005	0005	0005	0	0006	0034	0017	0	1	1	0	0	0		10
400	0005	0005	0000	0	0003	0037	0000	0	0	0	1	1	1		
401	0005	0005	0005	0	0007	0033	0000	0	0	0	1	1	1		01
402	0005	0005	0005	0	0007	0033	0001	0	0	0	1	1	0		01
403	0005	0005	0005	0	0007	0033	0003	0	0	0	1	1	0		01
404	0005	0005	0005	0	0007	0033	0007	0	0	0	1	1	0		00
405	0005	0005	0005	0	0007	0033	0016	0	0	1	1	1	0		10
406	0005	0005	0005	0	0007	0033	0014	0	0	1	1	1	0		10
407	0005	0005	0005	0	0007	0033	0010	0	0	1	1	1	0		10
408	0005	0005	0005	0	0007	0033	0000	0	0	0	1	1	1		01

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
409	0005	0005	0005	0	0007	0033	0001	0	0	0	1	1	0		00
410	0005	0005	0005	0	0007	0033	0002	0	0	0	1	1	0		01
411	0005	0005	0005	0	0007	0033	0005	0	0	0	1	1	0		00
412	0005	0005	0005	0	0007	0033	0012	0	0	1	1	1	0		10
413	0005	0005	0005	0	0007	0033	0004	0	0	0	1	1	0		01
414	0005	0005	0005	0	0007	0033	0011	0	0	1	1	1	0		11
415	0005	0005	0005	0	0007	0033	0003	0	0	0	1	1	0		00
416	0005	0005	0005	0	0007	0033	0006	0	0	0	1	1	0		01
417	0005	0005	0005	0	0007	0033	0015	0	0	1	1	1	0		11
418	0005	0005	0005	0	0007	0033	0013	0	0	1	1	1	0		11
419	0005	0005	0005	0	0007	0033	0007	0	0	0	1	1	0		01
420	0005	0005	0005	0	0007	0033	0017	0	1	1	0	0	0		10
421	0006	0006	0000	0	0003	0037	0000	0	0	0	1	1	1		
422	0006	0006	0006	0	0004	0034	0000	0	0	0	1	1	1		10
423	0006	0006	0006	0	0004	0034	0010	0	0	1	1	1	0		10
424	0006	0006	0006	0	0004	0034	0014	0	0	1	1	1	0		10
425	0006	0006	0006	0	0004	0034	0016	0	0	1	1	1	0		00
426	0006	0006	0006	0	0004	0034	0007	0	0	0	1	1	0		01
427	0006	0006	0006	0	0004	0034	0003	0	0	0	1	1	0		01
428	0006	0006	0006	0	0004	0034	0001	0	0	0	1	1	0		01
429	0006	0006	0006	0	0004	0034	0000	0	0	0	1	1	1		10
430	0006	0006	0006	0	0004	0034	0010	0	0	1	1	1	0		00
431	0006	0006	0006	0	0004	0034	0004	0	0	0	1	1	0		10
432	0006	0006	0006	0	0004	0034	0012	0	0	1	1	1	0		00
433	0006	0006	0006	0	0004	0034	0005	0	0	0	1	1	0		01
434	0006	0006	0006	0	0004	0034	0002	0	0	0	1	1	0		10
435	0006	0006	0006	0	0004	0034	0011	0	0	1	1	1	0		11
436	0006	0006	0006	0	0004	0034	0014	0	0	1	1	1	0		00
437	0006	0006	0006	0	0004	0034	0006	0	0	0	1	1	0		10
438	0006	0006	0006	0	0004	0034	0013	0	0	1	1	1	0		11
439	0006	0006	0006	0	0004	0034	0015	0	0	1	1	1	0		11
440	0006	0006	0006	0	0004	0034	0016	0	0	1	1	1	0		10
441	0006	0006	0006	0	0004	0034	0017	0	1	1	0	0	0		01
442	0006	0006	0000	0	0003	0037	0000	0	0	0	1	1	1		

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	C_{N+4}	OVR	F_0	Q_{3-0}	R_{3-0}
443	0006	0006	0006	0	0005	0033	0000	0	0	0	1	1	1		10
444	0006	0006	0006	0	0005	0033	0010	0	0	1	1	1	0		10
445	0006	0006	0006	0	0005	0033	0014	0	0	1	1	1	0		10
446	0006	0006	0006	0	0005	0033	0016	0	0	1	1	1	0		00
447	0006	0006	0006	0	0005	0033	0007	0	0	0	1	1	0		01
448	0006	0006	0006	0	0005	0033	0003	0	0	0	1	1	0		01
449	0006	0006	0006	0	0005	0033	0001	0	0	0	1	1	0		01
450	0006	0006	0006	0	0005	0033	0000	0	0	0	1	1	1		10
451	0006	0006	0006	0	0005	0033	0010	0	0	1	1	1	0		00
452	0006	0006	0006	0	0005	0033	0004	0	0	0	1	1	0		10
453	0006	0006	0006	0	0005	0033	0012	0	0	1	1	1	0		00
454	0006	0006	0006	0	0005	0033	0005	0	0	0	1	1	0		01
455	0006	0006	0006	0	0005	0033	0002	0	0	0	1	1	0		10
456	0006	0006	0006	0	0005	0033	0011	0	0	1	1	1	0		11
457	0006	0006	0006	0	0005	0033	0014	0	0	1	1	1	0		00
458	0006	0006	0006	0	0005	0033	0006	0	0	0	1	1	0		10
459	0006	0006	0006	0	0005	0033	0013	0	0	1	1	1	0		11
460	0006	0006	0006	0	0005	0033	0015	0	0	1	1	1	0		11
461	0006	0006	0006	0	0005	0033	0016	0	0	1	1	1	0		10
462	0006	0006	0006	0	0005	0033	0017	0	1	1	0	0	0		01
463	0006	0006	0000	0	0003	0037	0000	0	0	0	1	1	1		
464	0006	0006	0006	0	0006	0034	0000	0	0	0	1	1	1		01
465	0006	0006	0006	0	0006	0034	0001	0	0	0	1	1	0		01
466	0006	0006	0006	0	0006	0034	0003	0	0	0	1	1	0		01
467	0006	0006	0006	0	0006	0034	0007	0	0	0	1	1	0		00
468	0006	0006	0006	0	0006	0034	0016	0	0	1	1	1	0		10
469	0006	0006	0006	0	0006	0034	0014	0	0	1	1	1	0		10
470	0006	0006	0006	0	0006	0034	0010	0	0	1	1	1	0		10
471	0006	0006	0006	0	0006	0034	0000	0	0	0	1	1	1		01
472	0006	0006	0006	0	0006	0034	0001	0	0	0	1	1	0		00
473	0006	0006	0006	0	0006	0034	0002	0	0	0	1	1	0		01
474	0006	0006	0006	0	0006	0034	0005	0	0	0	1	1	0		00
475	0006	0006	0006	0	0006	0034	0012	0	0	1	1	1	0		10
476	0006	0006	0006	0	0006	0034	0004	0	0	0	1	1	0		01

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
477	0006	0006	0006	0	0006	0034	0011	0	0	1	1	1	0		11
478	0006	0006	0006	0	0006	0034	0003	0	0	0	1	1	0		00
479	0006	0006	0006	0	0006	0034	0006	0	0	0	1	1	0		01
480	0006	0006	0006	0	0006	0034	0015	0	0	1	1	1	0		11
481	0006	0006	0006	0	0006	0034	0013	0	0	1	1	1	0		11
482	0006	0006	0006	0	0006	0034	0007	0	0	0	1	1	0		01
483	0006	0006	0006	0	0006	0034	0017	0	1	1	0	0	0		10
484	0006	0006	0000	0	0003	0037	0000	0	0	0	1	1	1		
485	0006	0006	0006	0	0007	0033	0000	0	0	0	1	1	1		01
486	0006	0006	0006	0	0007	0033	0001	0	0	0	1	1	0		01
487	0006	0006	0006	0	0007	0033	0003	0	0	0	1	1	0		01
488	0006	0006	0006	0	0007	0033	0007	0	0	0	1	1	0		00
489	0006	0006	0006	0	0007	0033	0016	0	0	1	1	1	0		10
490	0006	0006	0006	0	0007	0033	0014	0	0	1	1	1	0		10
491	0006	0006	0006	0	0007	0033	0010	0	0	1	1	1	0		10
492	0006	0006	0006	0	0007	0033	0000	0	0	0	1	1	1		01
493	0006	0006	0006	0	0007	0033	0001	0	0	0	1	1	0		00
494	0006	0006	0006	0	0007	0033	0002	0	0	0	1	1	0		01
495	0006	0006	0006	0	0007	0033	0005	0	0	0	1	1	0		00
496	0006	0006	0006	0	0007	0033	0012	0	0	1	1	1	0		10
497	0006	0006	0006	0	0007	0033	0004	0	0	0	1	1	0		01
498	0006	0006	0006	0	0007	0033	0011	0	0	1	1	1	0		11
499	0006	0006	0006	0	0007	0033	0003	0	0	0	1	1	0		00
500	0006	0006	0006	0	0007	0033	0006	0	0	0	1	1	0		01
501	0006	0006	0006	0	0007	0033	0015	0	0	1	1	1	0		11
502	0006	0006	0006	0	0007	0033	0013	0	0	1	1	1	0		11
503	0006	0006	0006	0	0007	0033	0007	0	0	0	1	1	0		01
504	0006	0006	0006	0	0007	0033	0017	0	1	1	0	0	0		10
505	0007	0007	0000	0	0003	0037	0000	0	0	0	1	1	1		
506	0007	0007	0007	0	0004	0034	0000	0	0	0	1	1	1		10
507	0007	0007	0007	0	0004	0034	0010	0	0	1	1	1	0		10
508	0007	0007	0007	0	0004	0034	0014	0	0	1	1	1	0		10
509	0007	0007	0007	0	0004	0034	0016	0	0	1	1	1	0		00
510	0007	0007	0007	0	0004	0034	0007	0	0	0	1	1	0		01

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	G_{30}	P_{30}
511	0007	0007	0007	0	0004	0034	0003	0	0	0	1	1	0		01
512	0007	0007	0007	0	0004	0034	0001	0	0	0	1	1	0		01
513	0007	0007	0007	0	0004	0034	0000	0	0	0	1	1	1		10
514	0007	0007	0007	0	0004	0034	0010	0	0	1	1	1	0		00
515	0007	0007	0007	0	0004	0034	0004	0	0	0	1	1	0		10
516	0007	0007	0007	0	0004	0034	0012	0	0	1	1	1	0		00
517	0007	0007	0007	0	0004	0034	0005	0	0	0	1	1	0		01
518	0007	0007	0007	0	0004	0034	0002	0	0	0	1	1	0		10
519	0007	0007	0007	0	0004	0034	0011	0	0	1	1	1	0		11
520	0007	0007	0007	0	0004	0034	0014	0	0	1	1	1	0		00
521	0007	0007	0007	0	0004	0034	0006	0	0	0	1	1	0		10
522	0007	0007	0007	0	0004	0034	0013	0	0	1	1	1	0		11
523	0007	0007	0007	0	0004	0034	0015	0	0	1	1	1	0		11
524	0007	0007	0007	0	0004	0034	0016	0	0	1	1	1	0		10
525	0007	0007	0007	0	0004	0034	0017	0	1	1	0	0	0		01
526	0007	0007	0000	0	0003	0037	0000	0	0	0	1	1	1		
527	0007	0007	0007	0	0005	0033	0000	0	0	0	1	1	1		10
528	0007	0007	0007	0	0005	0033	0010	0	0	1	1	1	0		10
529	0007	0007	0007	0	0005	0033	0014	0	0	1	1	1	0		10
530	0007	0007	0007	0	0005	0033	0016	0	0	1	1	1	0		00
531	0007	0007	0007	0	0005	0033	0007	0	0	0	1	1	0		01
532	0007	0007	0007	0	0005	0033	0003	0	0	0	1	1	0		01
533	0007	0007	0007	0	0005	0033	0001	0	0	0	1	1	0		01
534	0007	0007	0007	0	0005	0033	0000	0	0	0	1	1	1		10
535	0007	0007	0007	0	0005	0033	0010	0	0	1	1	1	0		00
536	0007	0007	0007	0	0005	0033	0004	0	0	0	1	1	0		10
537	0007	0007	0007	0	0005	0033	0012	0	0	1	1	1	0		00
538	0007	0007	0007	0	0005	0033	0005	0	0	0	1	1	0		01
539	0007	0007	0007	0	0005	0033	0002	0	0	0	1	1	0		10
540	0007	0007	0007	0	0005	0033	0011	0	0	1	1	1	0		11
541	0007	0007	0007	0	0005	0033	0014	0	0	1	1	1	0		00
542	0007	0007	0007	0	0005	0033	0006	0	0	0	1	1	0		10
543	0007	0007	0007	0	0005	0033	0013	0	0	1	1	1	0		11
544	0007	0007	0007	0	0005	0033	0015	0	0	1	1	1	0		11

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
545	0007	0007	0007	0	0005	0033	0016	0	0	1	1	1	0		10
546	0007	0007	0007	0	0005	0033	0017	0	1	1	0	0	0		01
547	0007	0007	0000	0	0003	0037	0000	0	0	0	1	1	1		
548	0007	0007	0007	0	0006	0034	0000	0	0	0	1	1	1		01
549	0007	0007	0007	0	0006	0034	0001	0	0	0	1	1	0		01
550	0007	0007	0007	0	0006	0034	0003	0	0	0	1	1	0		01
551	0007	0007	0007	0	0006	0034	0007	0	0	0	1	1	0		00
552	0007	0007	0007	0	0006	0034	0016	0	0	1	1	1	0		10
553	0007	0007	0007	0	0006	0034	0014	0	0	1	1	1	0		10
554	0007	0007	0007	0	0006	0034	0010	0	0	1	1	1	0		10
555	0007	0007	0007	0	0006	0034	0000	0	0	0	1	1	1		01
556	0007	0007	0007	0	0006	0034	0001	0	0	0	1	1	0		00
557	0007	0007	0007	0	0006	0034	0002	0	0	0	1	1	0		01
558	0007	0007	0007	0	0006	0034	0005	0	0	0	1	1	0		00
559	0007	0007	0007	0	0006	0034	0012	0	0	1	1	1	0		10
560	0007	0007	0007	0	0006	0034	0004	0	0	0	1	1	0		01
561	0007	0007	0007	0	0006	0034	0011	0	0	1	1	1	0		11
562	0007	0007	0007	0	0006	0034	0003	0	0	0	1	1	0		00
563	0007	0007	0007	0	0006	0034	0006	0	0	0	1	1	0		01
564	0007	0007	0007	0	0006	0034	0015	0	0	1	1	1	0		11
565	0007	0007	0007	0	0006	0034	0013	0	0	1	1	1	0		11
566	0007	0007	0007	0	0006	0034	0007	0	0	0	1	1	0		01
567	0007	0007	0007	0	0006	0034	0017	0	1	1	0	0	0		10
568	0007	0007	0000	0	0003	0037	0000	0	0	0	1	1	1		
569	0007	0007	0007	0	0007	0033	0000	0	0	0	1	1	1		01
570	0007	0007	0007	0	0007	0033	0001	0	0	0	1	1	0		01
571	0007	0007	0007	0	0007	0033	0003	0	0	0	1	1	0		01
572	0007	0007	0007	0	0007	0033	0007	0	0	0	1	1	0		00
573	0007	0007	0007	0	0007	0033	0016	0	0	1	1	1	0		10
574	0007	0007	0007	0	0007	0033	0014	0	0	1	1	1	0		10
575	0007	0007	0007	0	0007	0033	0010	0	0	1	1	1	0		10
576	0007	0007	0007	0	0007	0033	0000	0	0	0	1	1	1		01
577	0007	0007	0007	0	0007	0033	0001	0	0	0	1	1	0		00
578	0007	0007	0007	0	0007	0033	0002	0	0	0	1	1	0		01

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
579	0007	0007	0007	0	0007	0033	0005	0	0	0	1	1	0		00
580	0007	0007	0007	0	0007	0033	0012	0	0	1	1	1	0		10
581	0007	0007	0007	0	0007	0033	0004	0	0	0	1	1	0		01
582	0007	0007	0007	0	0007	0033	0011	0	0	1	1	1	0		11
583	0007	0007	0007	0	0007	0033	0003	0	0	0	1	1	0		00
584	0007	0007	0007	0	0007	0033	0006	0	0	0	1	1	0		01
585	0007	0007	0007	0	0007	0033	0015	0	0	1	1	1	0		11
586	0007	0007	0007	0	0007	0033	0013	0	0	1	1	1	0		11
587	0007	0007	0007	0	0007	0033	0007	0	0	0	1	1	0		01
588	0007	0007	0007	0	0007	0033	0017	0	1	1	0	0	0		10
589	0010	0010	0000	0	0003	0037	0000	0	0	0	1	1	1		
590	0010	0010	0010	0	0004	0034	0000	0	0	0	1	1	1		10
591	0010	0010	0010	0	0004	0034	0010	0	0	1	1	1	0		10
592	0010	0010	0010	0	0004	0034	0014	0	0	1	1	1	0		10
593	0010	0010	0010	0	0004	0034	0016	0	0	1	1	1	0		00
594	0010	0010	0010	0	0004	0034	0007	0	0	0	1	1	0		01
595	0010	0010	0010	0	0004	0034	0003	0	0	0	1	1	0		01
596	0010	0010	0010	0	0004	0034	0001	0	0	0	1	1	0		01
597	0010	0010	0010	0	0004	0034	0000	0	0	0	1	1	1		10
598	0010	0010	0010	0	0004	0034	0010	0	0	1	1	1	0		00
599	0010	0010	0010	0	0004	0034	0004	0	0	0	1	1	0		10
600	0010	0010	0010	0	0004	0034	0012	0	0	1	1	1	0		00
601	0010	0010	0010	0	0004	0034	0005	0	0	0	1	1	0		01
602	0010	0010	0010	0	0004	0034	0002	0	0	0	1	1	0		10
603	0010	0010	0010	0	0004	0034	0011	0	0	1	1	1	0		11
604	0010	0010	0010	0	0004	0034	0014	0	0	1	1	1	0		00
605	0010	0010	0010	0	0004	0034	0006	0	0	0	1	1	0		10
606	0010	0010	0010	0	0004	0034	0013	0	0	1	1	1	0		11
607	0010	0010	0010	0	0004	0034	0015	0	0	1	1	1	0		11
608	0010	0010	0010	0	0004	0034	0016	0	0	1	1	1	0		10
609	0010	0010	0010	0	0004	0034	0017	0	1	1	0	0	0		01
610	0010	0010	0000	0	0003	0037	0000	0	0	0	1	1	1		
611	0010	0010	0010	0	0005	0033	0000	0	0	0	1	1	1		10
612	0010	0010	0010	0	0005	0033	0010	0	0	1	1	1	0		10

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
613	0010	0010	0010	0	0005	0033	0014	0	0	1	1	1	0		10
614	0010	0010	0010	0	0005	0033	0016	0	0	1	1	1	0		00
615	0010	0010	0010	0	0005	0033	0007	0	0	0	1	1	0		01
616	0010	0010	0010	0	0005	0033	0003	0	0	0	1	1	0		01
617	0010	0010	0010	0	0005	0033	0001	0	0	0	1	1	0		01
618	0010	0010	0010	0	0005	0033	0000	0	0	0	1	1	1		10
619	0010	0010	0010	0	0005	0033	0010	0	0	1	1	1	0		00
620	0010	0010	0010	0	0005	0033	0004	0	0	0	1	1	0		10
621	0010	0010	0010	0	0005	0033	0012	0	0	1	1	1	0		00
622	0010	0010	0010	0	0005	0033	0005	0	0	0	1	1	0		01
623	0010	0010	0010	0	0005	0033	0002	0	0	0	1	1	0		10
624	0010	0010	0010	0	0005	0033	0011	0	0	1	1	1	0		11
625	0010	0010	0010	0	0005	0033	0014	0	0	1	1	1	0		00
626	0010	0010	0010	0	0005	0033	0006	0	0	0	1	1	0		10
627	0010	0010	0010	0	0005	0033	0013	0	0	1	1	1	0		11
628	0010	0010	0010	0	0005	0033	0015	0	0	1	1	1	0		11
629	0010	0010	0010	0	0005	0033	0016	0	0	1	1	1	0		10
630	0010	0010	0010	0	0005	0033	0017	0	1	1	0	0	0		01
631	0010	0010	0000	0	0003	0037	0000	0	0	0	1	1	1		
632	0010	0010	0010	0	0006	0034	0000	0	0	0	1	1	1		01
633	0010	0010	0010	0	0006	0034	0001	0	0	0	1	1	0		01
634	0010	0010	0010	0	0006	0034	0003	0	0	0	1	1	0		01
635	0010	0010	0010	0	0006	0034	0007	0	0	0	1	1	0		00
636	0010	0010	0010	0	0006	0034	0016	0	0	1	1	1	0		10
637	0010	0010	0010	0	0006	0034	0014	0	0	1	1	1	0		10
638	0010	0010	0010	0	0006	0034	0010	0	0	1	1	1	0		10
639	0010	0010	0010	0	0006	0034	0000	0	0	0	1	1	1		01
640	0010	0010	0010	0	0006	0034	0001	0	0	0	1	1	0		00
641	0010	0010	0010	0	0006	0034	0002	0	0	0	1	1	0		01
642	0010	0010	0010	0	0006	0034	0005	0	0	0	1	1	0		00
643	0010	0010	0010	0	0006	0034	0012	0	0	1	1	1	0		10
644	0010	0010	0010	0	0006	0034	0004	0	0	0	1	1	0		01
645	0010	0010	0010	0	0006	0034	0011	0	0	1	1	1	0		11
646	0010	0010	0010	0	0006	0034	0003	0	0	0	1	1	0		00

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
647	0010	0010	0010	0	0006	0034	0006	0	0	0	1	1	0		01
648	0010	0010	0010	0	0006	0034	0015	0	0	1	1	1	0		11
649	0010	0010	0010	0	0006	0034	0013	0	0	1	1	1	0		11
650	0010	0010	0010	0	0006	0034	0007	0	0	0	1	1	0		01
651	0010	0010	0010	0	0006	0034	0017	0	1	1	0	0	0		10
652	0010	0010	0000	0	0003	0037	0000	0	0	0	1	1	1		
653	0010	0010	0010	0	0007	0033	0000	0	0	0	1	1	1		01
654	0010	0010	0010	0	0007	0033	0001	0	0	0	1	1	0		01
655	0010	0010	0010	0	0007	0033	0003	0	0	0	1	1	0		01
656	0010	0010	0010	0	0007	0033	0007	0	0	0	1	1	0		00
657	0010	0010	0010	0	0007	0033	0016	0	0	1	1	1	0		10
658	0010	0010	0010	0	0007	0033	0014	0	0	1	1	1	0		10
659	0010	0010	0010	0	0007	0033	0010	0	0	1	1	1	0		10
660	0010	0010	0010	0	0007	0033	0000	0	0	0	1	1	1		01
661	0010	0010	0010	0	0007	0033	0001	0	0	0	1	1	0		00
662	0010	0010	0010	0	0007	0033	0002	0	0	0	1	1	0		01
663	0010	0010	0010	0	0007	0033	0005	0	0	0	1	1	0		00
664	0010	0010	0010	0	0007	0033	0012	0	0	1	1	1	0		10
665	0010	0010	0010	0	0007	0033	0004	0	0	0	1	1	0		01
666	0010	0010	0010	0	0007	0033	0011	0	0	1	1	1	0		11
667	0010	0010	0010	0	0007	0033	0003	0	0	0	1	1	0		00
668	0010	0010	0010	0	0007	0033	0006	0	0	0	1	1	0		01
669	0010	0010	0010	0	0007	0033	0015	0	0	1	1	1	0		11
670	0010	0010	0010	0	0007	0033	0013	0	0	1	1	1	0		11
671	0010	0010	0010	0	0007	0033	0007	0	0	0	1	1	0		01
672	0010	0010	0010	0	0007	0033	0017	0	1	1	0	0	0		10
673	0011	0011	0000	0	0003	0037	0000	0	0	0	1	1	1		
674	0011	0011	0011	0	0004	0034	0000	0	0	0	1	1	1		10
675	0011	0011	0011	0	0004	0034	0010	0	0	1	1	1	0		10
676	0011	0011	0011	0	0004	0034	0014	0	0	1	1	1	0		10
677	0011	0011	0011	0	0004	0034	0016	0	0	1	1	1	0		00
678	0011	0011	0011	0	0004	0034	0007	0	0	0	1	1	0		01
679	0011	0011	0011	0	0004	0034	0003	0	0	0	1	1	0		01
680	0011	0011	0011	0	0004	0034	0001	0	0	0	1	1	0		01

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
681	0011	0011	0011	0	0004	0034	0000	0	0	0	1	1	1		10
682	0011	0011	0011	0	0004	0034	0010	0	0	1	1	1	0		00
683	0011	0011	0011	0	0004	0034	0004	0	0	0	1	1	0		10
684	0011	0011	0011	0	0004	0034	0012	0	0	1	1	1	0		00
685	0011	0011	0011	0	0004	0034	0005	0	0	0	1	1	0		01
686	0011	0011	0011	0	0004	0034	0002	0	0	0	1	1	0		10
687	0011	0011	0011	0	0004	0034	0011	0	0	1	1	1	0		11
688	0011	0011	0011	0	0004	0034	0014	0	0	1	1	1	0		00
689	0011	0011	0011	0	0004	0034	0006	0	0	0	1	1	0		10
690	0011	0011	0011	0	0004	0034	0013	0	0	1	1	1	0		11
691	0011	0011	0011	0	0004	0034	0015	0	0	1	1	1	0		11
692	0011	0011	0011	0	0004	0034	0016	0	0	1	1	1	0		10
693	0011	0011	0011	0	0004	0034	0017	0	1	1	0	0	0		01
694	0011	0011	0000	0	0003	0037	0000	0	0	0	1	1	1		
695	0011	0011	0011	0	0005	0033	0000	0	0	0	1	1	1		10
696	0011	0011	0011	0	0005	0033	0010	0	0	1	1	1	0		10
697	0011	0011	0011	0	0005	0033	0014	0	0	1	1	1	0		10
698	0011	0011	0011	0	0005	0033	0016	0	0	1	1	1	0		00
699	0011	0011	0011	0	0005	0033	0007	0	0	0	1	1	0		01
700	0011	0011	0011	0	0005	0033	0003	0	0	0	1	1	0		01
701	0011	0011	0011	0	0005	0033	0001	0	0	0	1	1	0		01
702	0011	0011	0011	0	0005	0033	0000	0	0	0	1	1	1		10
703	0011	0011	0011	0	0005	0033	0010	0	0	1	1	1	0		00
704	0011	0011	0011	0	0005	0033	0004	0	0	0	1	1	0		10
705	0011	0011	0011	0	0005	0033	0012	0	0	1	1	1	0		00
706	0011	0011	0011	0	0005	0033	0005	0	0	0	1	1	0		01
707	0011	0011	0011	0	0005	0033	0002	0	0	0	1	1	0		10
708	0011	0011	0011	0	0005	0033	0011	0	0	1	1	1	0		11
709	0011	0011	0011	0	0005	0033	0014	0	0	1	1	1	0		00
710	0011	0011	0011	0	0005	0033	0006	0	0	0	1	1	0		10
711	0011	0011	0011	0	0005	0033	0013	0	0	1	1	1	0		11
712	0011	0011	0011	0	0005	0033	0015	0	0	1	1	1	0		11
713	0011	0011	0011	0	0005	0033	0016	0	0	1	1	1	0		10
714	0011	0011	0011	0	0005	0033	0017	0	1	1	0	0	0		01

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
715	0011	0011	0000	0	0003	0037	0000	0	0	0	1	1	1		
716	0011	0011	0011	0	0006	0034	0000	0	0	0	1	1	1		01
717	0011	0011	0011	0	0006	0034	0001	0	0	0	1	1	0		01
718	0011	0011	0011	0	0006	0034	0003	0	0	0	1	1	0		01
719	0011	0011	0011	0	0006	0034	0007	0	0	0	1	1	0		00
720	0011	0011	0011	0	0006	0034	0016	0	0	1	1	1	0		10
721	0011	0011	0011	0	0006	0034	0014	0	0	1	1	1	0		10
722	0011	0011	0011	0	0006	0034	0010	0	0	1	1	1	0		10
723	0011	0011	0011	0	0006	0034	0000	0	0	0	1	1	1		01
724	0011	0011	0011	0	0006	0034	0001	0	0	0	1	1	0		00
725	0011	0011	0011	0	0006	0034	0002	0	0	0	1	1	0		01
726	0011	0011	0011	0	0006	0034	0005	0	0	0	1	1	0		00
727	0011	0011	0011	0	0006	0034	0012	0	0	1	1	1	0		10
728	0011	0011	0011	0	0006	0034	0004	0	0	0	1	1	0		01
729	0011	0011	0011	0	0006	0034	0011	0	0	1	1	1	0		11
730	0011	0011	0011	0	0006	0034	0003	0	0	0	1	1	0		00
731	0011	0011	0011	0	0006	0034	0006	0	0	0	1	1	0		01
732	0011	0011	0011	0	0006	0034	0015	0	0	1	1	1	0		11
733	0011	0011	0011	0	0006	0034	0013	0	0	1	1	1	0		11
734	0011	0011	0011	0	0006	0034	0007	0	0	0	1	1	0		01
735	0011	0011	0011	0	0006	0034	0017	0	1	1	0	0	0		10
736	0011	0011	0000	0	0003	0037	0000	0	0	0	1	1	1		
737	0011	0011	0011	0	0007	0033	0000	0	0	0	1	1	1		01
738	0011	0011	0011	0	0007	0033	0001	0	0	0	1	1	0		01
739	0011	0011	0011	0	0007	0033	0003	0	0	0	1	1	0		01
740	0011	0011	0011	0	0007	0033	0007	0	0	0	1	1	0		00
741	0011	0011	0011	0	0007	0033	0016	0	0	1	1	1	0		10
742	0011	0011	0011	0	0007	0033	0014	0	0	1	1	1	0		10
743	0011	0011	0011	0	0007	0033	0010	0	0	1	1	1	0		10
744	0011	0011	0011	0	0007	0033	0000	0	0	0	1	1	1		01
745	0011	0011	0011	0	0007	0033	0001	0	0	0	1	1	0		00
746	0011	0011	0011	0	0007	0033	0002	0	0	0	1	1	0		01
747	0011	0011	0011	0	0007	0033	0005	0	0	0	1	1	0		00
748	0011	0011	0011	0	0007	0033	0012	0	0	1	1	1	0		10

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
749	0011	0011	0011	0	0007	0033	0004	0	0	0	1	1	0		01
750	0011	0011	0011	0	0007	0033	0011	0	0	1	1	1	0		11
751	0011	0011	0011	0	0007	0033	0003	0	0	0	1	1	0		00
752	0011	0011	0011	0	0007	0033	0006	0	0	0	1	1	0		01
753	0011	0011	0011	0	0007	0033	0015	0	0	1	1	1	0		11
754	0011	0011	0011	0	0007	0033	0013	0	0	1	1	1	0		11
755	0011	0011	0011	0	0007	0033	0007	0	0	0	1	1	0		01
756	0011	0011	0011	0	0007	0033	0017	0	1	1	0	0	0		10
757	0012	0012	0000	0	0003	0037	0000	0	0	0	1	1	1		
758	0012	0012	0012	0	0004	0034	0000	0	0	0	1	1	1		10
759	0012	0012	0012	0	0004	0034	0010	0	0	1	1	1	0		10
760	0012	0012	0012	0	0004	0034	0014	0	0	1	1	1	0		10
761	0012	0012	0012	0	0004	0034	0016	0	0	1	1	1	0		00
762	0012	0012	0012	0	0004	0034	0007	0	0	0	1	1	0		01
763	0012	0012	0012	0	0004	0034	0003	0	0	0	1	1	0		01
764	0012	0012	0012	0	0004	0034	0001	0	0	0	1	1	0		01
765	0012	0012	0012	0	0004	0034	0000	0	0	0	1	1	1		10
766	0012	0012	0012	0	0004	0034	0010	0	0	1	1	1	0		00
767	0012	0012	0012	0	0004	0034	0004	0	0	0	1	1	0		10
768	0012	0012	0012	0	0004	0034	0012	0	0	1	1	1	0		00
769	0012	0012	0012	0	0004	0034	0005	0	0	0	1	1	0		01
770	0012	0012	0012	0	0004	0034	0002	0	0	0	1	1	0		10
771	0012	0012	0012	0	0004	0034	0011	0	0	1	1	1	0		11
772	0012	0012	0012	0	0004	0034	0014	0	0	1	1	1	0		00
773	0012	0012	0012	0	0004	0034	0006	0	0	0	1	1	0		10
774	0012	0012	0012	0	0004	0034	0013	0	0	1	1	1	0		11
775	0012	0012	0012	0	0004	0034	0015	0	0	1	1	1	0		11
776	0012	0012	0012	0	0004	0034	0016	0	0	1	1	1	0		10
777	0012	0012	0012	0	0004	0034	0017	0	1	1	0	0	0		01
778	0012	0012	0000	0	0003	0037	0000	0	0	0	1	1	1		
779	0012	0012	0012	0	0005	0033	0000	0	0	0	1	1	1		10
780	0012	0012	0012	0	0005	0033	0010	0	0	1	1	1	0		10
781	0012	0012	0012	0	0005	0033	0014	0	0	1	1	1	0		10
782	0012	0012	0012	0	0005	0033	0016	0	0	1	1	1	0		00

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
783	0012	0012	0012	0	0005	0033	0007	0	0	0	1	1	0		01
784	0012	0012	0012	0	0005	0033	0003	0	0	0	1	1	0		01
785	0012	0012	0012	0	0005	0033	0001	0	0	0	1	1	0		01
786	0012	0012	0012	0	0005	0033	0000	0	0	0	1	1	1		10
787	0012	0012	0012	0	0005	0033	0010	0	0	1	1	1	0		00
788	0012	0012	0012	0	0005	0033	0004	0	0	0	1	1	0		10
789	0012	0012	0012	0	0005	0033	0012	0	0	1	1	1	0		00
790	0012	0012	0012	0	0005	0033	0005	0	0	0	1	1	0		01
791	0012	0012	0012	0	0005	0033	0002	0	0	0	1	1	0		10
792	0012	0012	0012	0	0005	0033	0011	0	0	1	1	1	0		11
793	0012	0012	0012	0	0005	0033	0014	0	0	1	1	1	0		00
794	0012	0012	0012	0	0005	0033	0006	0	0	0	1	1	0		10
795	0012	0012	0012	0	0005	0033	0013	0	0	1	1	1	0		11
796	0012	0012	0012	0	0005	0033	0015	0	0	1	1	1	0		11
797	0012	0012	0012	0	0005	0033	0016	0	0	1	1	1	0		10
798	0012	0012	0012	0	0005	0033	0017	0	1	1	0	0	0		01
799	0012	0012	0000	0	0003	0037	0000	0	0	0	1	1	1		
800	0012	0012	0012	0	0006	0034	0000	0	0	0	1	1	1		01
801	0012	0012	0012	0	0006	0034	0001	0	0	0	1	1	0		01
802	0012	0012	0012	0	0006	0034	0003	0	0	0	1	1	0		01
803	0012	0012	0012	0	0006	0034	0007	0	0	0	1	1	0		00
804	0012	0012	0012	0	0006	0034	0016	0	0	1	1	1	0		10
805	0012	0012	0012	0	0006	0034	0014	0	0	1	1	1	0		10
806	0012	0012	0012	0	0006	0034	0010	0	0	1	1	1	0		10
807	0012	0012	0012	0	0006	0034	0000	0	0	0	1	1	1		01
808	0012	0012	0012	0	0006	0034	0001	0	0	0	1	1	0		00
809	0012	0012	0012	0	0006	0034	0002	0	0	0	1	1	0		01
810	0012	0012	0012	0	0006	0034	0005	0	0	0	1	1	0		00
811	0012	0012	0012	0	0006	0034	0012	0	0	1	1	1	0		10
812	0012	0012	0012	0	0006	0034	0004	0	0	0	1	1	0		01
813	0012	0012	0012	0	0006	0034	0011	0	0	1	1	1	0		11
814	0012	0012	0012	0	0006	0034	0003	0	0	0	1	1	0		01
815	0012	0012	0012	0	0006	0034	0006	0	0	0	1	1	0		11
816	0012	0012	0012	0	0006	0034	0015	0	0	1	1	1	0		11

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
817	0012	0012	0012	0	0006	0034	0013	0	0	1	1	1	0		11
818	0012	0012	0012	0	0006	0034	0007	0	0	0	1	1	0		01
819	0012	0012	0012	0	0006	0034	0017	0	1	1	0	0	0		10
820	0012	0012	0000	0	0003	0037	0000	0	0	0	1	1	1		
821	0012	0012	0012	0	0007	0033	0000	0	0	0	1	1	1		01
822	0012	0012	0012	0	0007	0033	0001	0	0	0	1	1	0		01
823	0012	0012	0012	0	0007	0033	0003	0	0	0	1	1	0		01
824	0012	0012	0012	0	0007	0033	0007	0	0	0	1	1	0		00
825	0012	0012	0012	0	0007	0033	0016	0	0	1	1	1	0		10
826	0012	0012	0012	0	0007	0033	0014	0	0	1	1	1	0		10
827	0012	0012	0012	0	0007	0033	0010	0	0	1	1	1	0		10
828	0012	0012	0012	0	0007	0033	0000	0	0	0	1	1	1		01
829	0012	0012	0012	0	0007	0033	0001	0	0	0	1	1	0		00
830	0012	0012	0012	0	0007	0033	0002	0	0	0	1	1	0		01
831	0012	0012	0012	0	0007	0033	0005	0	0	0	1	1	0		00
832	0012	0012	0012	0	0007	0033	0012	0	0	1	1	1	0		10
833	0012	0012	0012	0	0007	0033	0004	0	0	0	1	1	0		01
834	0012	0012	0012	0	0007	0033	0011	0	0	1	1	1	0		11
835	0012	0012	0012	0	0007	0033	0003	0	0	0	1	1	0		00
836	0012	0012	0012	0	0007	0033	0006	0	0	0	1	1	0		01
837	0012	0012	0012	0	0007	0033	0015	0	0	1	1	1	0		11
838	0012	0012	0012	0	0007	0033	0013	0	0	1	1	1	0		11
839	0012	0012	0012	0	0007	0033	0007	0	0	0	1	1	0		01
840	0012	0012	0012	0	0007	0033	0017	0	1	1	0	0	0		10
841	0013	0013	0000	0	0003	0037	0000	0	0	0	1	1	1		
842	0013	0013	0013	0	0004	0034	0000	0	0	0	1	1	1		10
843	0013	0013	0013	0	0004	0034	0010	0	0	1	1	1	0		10
844	0013	0013	0013	0	0004	0034	0014	0	0	1	1	1	0		10
845	0013	0013	0013	0	0004	0034	0016	0	0	1	1	1	0		00
846	0013	0013	0013	0	0004	0034	0007	0	0	0	1	1	0		01
847	0013	0013	0013	0	0004	0034	0003	0	0	0	1	1	0		01
848	0013	0013	0013	0	0004	0034	0001	0	0	0	1	1	0		01
849	0013	0013	0013	0	0004	0034	0000	0	0	0	1	1	1		10
850	0013	0013	0013	0	0004	0034	0010	0	0	1	1	1	0		00

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
851	0013	0013	0013	0	0004	0034	0004	0	0	0	1	1	0		10
852	0013	0013	0013	0	0004	0034	0012	0	0	1	1	1	0		00
853	0013	0013	0013	0	0004	0034	0005	0	0	0	1	1	0		01
854	0013	0013	0013	0	0004	0034	0002	0	0	0	1	1	0		10
855	0013	0013	0013	0	0004	0034	0011	0	0	1	1	1	0		11
856	0013	0013	0013	0	0004	0034	0014	0	0	1	1	1	0		00
857	0013	0013	0013	0	0004	0034	0006	0	0	0	1	1	0		10
858	0013	0013	0013	0	0004	0034	0013	0	0	1	1	1	0		11
859	0013	0013	0013	0	0004	0034	0015	0	0	1	1	1	0		11
860	0013	0013	0013	0	0004	0034	0016	0	0	1	1	1	0		10
861	0013	0013	0013	0	0004	0034	0017	0	1	1	0	0	0		01
852	0013	0013	0000	0	0003	0037	0000	0	0	0	1	1	1		
863	0013	0013	0013	0	0005	0033	0000	0	0	0	1	1	1		10
864	0013	0013	0013	0	0005	0033	0010	0	0	1	1	1	0		10
865	0013	0013	0013	0	0005	0033	0014	0	0	1	1	1	0		10
866	0013	0013	0013	0	0005	0033	0016	0	0	1	1	1	0		00
867	0013	0013	0013	0	0005	0033	0007	0	0	0	1	1	0		01
868	0013	0013	0013	0	0005	0033	0003	0	0	0	1	1	0		01
869	0013	0013	0013	0	0005	0033	0001	0	0	0	1	1	0		01
870	0013	0013	0013	0	0005	0033	0000	0	0	0	1	1	1		10
871	0013	0013	0013	0	0005	0033	0010	0	0	1	1	1	0		00
872	0013	0013	0013	0	0005	0033	0004	0	0	0	1	1	0		10
873	0013	0013	0013	0	0005	0033	0012	0	0	1	1	1	0		00
874	0013	0013	0013	0	0005	0033	0005	0	0	0	1	1	0		01
875	0013	0013	0013	0	0005	0033	0002	0	0	0	1	1	0		10
876	0013	0013	0013	0	0005	0033	0011	0	0	1	1	1	0		11
877	0013	0013	0013	0	0005	0033	0014	0	0	1	1	1	0		00
878	0013	0013	0013	0	0005	0033	0006	0	0	0	1	1	0		10
879	0013	0013	0013	0	0005	0033	0013	0	0	1	1	1	0		11
880	0013	0013	0013	0	0005	0033	0015	0	0	1	1	1	0		11
881	0013	0013	0013	0	0005	0033	0016	0	0	1	1	1	0		10
882	0013	0013	0013	0	0005	0033	0017	0	1	1	0	0	0		01
883	0013	0013	0000	0	0003	0037	0000	0	0	0	1	1	1		
884	0013	0013	0013	0	0006	0034	0000	0	0	0	1	1	1		01

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
885	0013	0013	0013	0	0006	0034	0001	0	0	0	1	1	0		01
886	0013	0013	0013	0	0006	0034	0003	0	0	0	1	1	0		01
887	0013	0013	0013	0	0006	0034	0007	0	0	0	1	1	0		00
888	0013	0013	0013	0	0006	0034	0016	0	0	1	1	1	0		10
889	0013	0013	0013	0	0006	0034	0014	0	0	1	1	1	0		10
890	0013	0013	0013	0	0006	0034	0010	0	0	1	1	1	0		10
891	0013	0013	0013	0	0006	0034	0000	0	0	0	1	1	1		01
892	0013	0013	0013	0	0006	0034	0001	0	0	0	1	1	0		00
893	0013	0013	0013	0	0006	0034	0002	0	0	0	1	1	0		01
894	0013	0013	0013	0	0006	0034	0005	0	0	0	1	1	0		00
895	0013	0013	0013	0	0006	0034	0012	0	0	1	1	1	0		10
896	0013	0013	0013	0	0006	0034	0004	0	0	0	1	1	0		01
897	0013	0013	0013	0	0006	0034	0011	0	0	1	1	1	0		11
898	0013	0013	0013	0	0006	0034	0003	0	0	0	1	1	0		00
899	0013	0013	0013	0	0006	0034	0006	0	0	0	1	1	0		01
900	0013	0013	0013	0	0006	0034	0015	0	0	1	1	1	0		11
901	0013	0013	0013	0	0006	0034	0013	0	0	1	1	1	0		11
902	0013	0013	0013	0	0006	0034	0007	0	0	0	1	1	0		01
903	0013	0013	0013	0	0006	0034	0017	0	1	1	0	0	0		10
904	0013	0013	0000	0	0003	0037	0000	0	0	0	1	1	1		
905	0013	0013	0013	0	0007	0033	0000	0	0	0	1	1	1		01
906	0013	0013	0013	0	0007	0033	0001	0	0	0	1	1	0		01
907	0013	0013	0013	0	0007	0033	0003	0	0	0	1	1	0		01
908	0013	0013	0013	0	0007	0033	0007	0	0	0	1	1	0		00
909	0013	0013	0013	0	0007	0033	0016	0	0	1	1	1	0		10
910	0013	0013	0013	0	0007	0033	0014	0	0	1	1	1	0		10
911	0013	0013	0013	0	0007	0033	0010	0	0	1	1	1	0		10
912	0013	0013	0013	0	0007	0033	0000	0	0	0	1	1	1		01
913	0013	0013	0013	0	0007	0033	0001	0	0	0	1	1	0		00
914	0013	0013	0013	0	0007	0033	0002	0	0	0	1	1	0		01
915	0013	0013	0013	0	0007	0033	0005	0	0	0	1	1	0		00
916	0013	0013	0013	0	0007	0033	0012	0	0	1	1	1	0		10
917	0013	0013	0013	0	0007	0033	0004	0	0	0	1	1	0		01
918	0013	0013	0013	0	0007	0033	0011	0	0	1	1	1	0		11

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
919	0013	0013	0013	0	0007	0033	00 03	0	0	0	1	1	0		00
920	0013	0013	0013	0	0007	0033	00 06	0	0	0	1	1	0		01
921	0013	0013	0013	0	0007	0033	00 15	0	0	1	1	1	0		11
922	0013	0013	0013	0	0007	0033	00 13	0	0	1	1	1	0		11
923	0013	0013	0013	0	0007	0033	00 07	0	0	0	1	1	0		01
924	0013	0013	0013	0	0007	0033	00 17	0	1	1	0	0	0		10
925	0014	0014	0000	0	0003	0037	00 00	0	0	0	1	1	1		
926	0014	0014	0014	0	0004	0034	00 00	0	0	0	1	1	1		10
927	0014	0014	0014	0	0004	0034	00 10	0	0	1	1	1	0		10
928	0014	0014	0014	0	0004	0034	00 14	0	0	1	1	1	0		10
929	0014	0014	0014	0	0004	0034	00 16	0	0	1	1	1	0		00
930	0014	0014	0014	0	0004	0034	00 07	0	0	0	1	1	0		01
931	0014	0014	0014	0	0004	0034	00 03	0	0	0	1	1	0		01
932	0014	0014	0014	0	0004	0034	00 01	0	0	0	1	1	0		01
933	0014	0014	0014	0	0004	0034	00 00	0	0	0	1	1	1		10
934	0014	0014	0014	0	0004	0034	00 10	0	0	1	1	1	0		00
935	0014	0014	0014	0	0004	0034	00 04	0	0	0	1	1	0		10
936	0014	0014	0014	0	0004	0034	00 12	0	0	1	1	1	0		00
937	0014	0014	0014	0	0004	0034	00 05	0	0	0	1	1	0		01
938	0014	0014	0014	0	0004	0034	00 02	0	0	0	1	1	0		10
939	0014	0014	0014	0	0004	0034	00 11	0	0	1	1	1	0		11
940	0014	0014	0014	0	0004	0034	00 14	0	0	1	1	1	0		00
941	0014	0014	0014	0	0004	0034	00 06	0	0	0	1	1	0		10
942	0014	0014	0014	0	0004	0034	00 13	0	0	1	1	1	0		11
943	0014	0014	0014	0	0004	0034	00 15	0	0	1	1	1	0		11
944	0014	0014	0014	0	0004	0034	00 16	0	0	1	1	1	0		10
945	0014	0014	0014	0	0004	0034	00 17	0	1	1	0	0	0		01
946	0014	0014	0000	0	0003	0037	00 00	0	0	0	1	1	1		
947	0014	0014	0014	0	0005	0033	00 00	0	0	0	1	1	1		10
948	0014	0014	0014	0	0005	0033	00 10	0	0	1	1	1	0		10
949	0014	0014	0014	0	0005	0033	00 14	0	0	1	1	1	0		10
950	0014	0014	0014	0	0005	0033	00 16	0	0	1	1	1	0		00
951	0014	0014	0014	0	0005	0033	00 07	0	0	0	1	1	0		01
952	0014	0014	0014	0	0005	0033	00 03	0	0	0	1	1	0		01

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
953	0014	0014	0014	0	0005	0033	0001	0	0	0	1	1	0		01
954	0014	0014	0014	0	0005	0033	0000	0	0	0	1	1	1		10
955	0014	0014	0014	0	0005	0033	0010	0	0	1	1	1	0		00
956	0014	0014	0014	0	0005	0033	0004	0	0	0	1	1	0		10
957	0014	0014	0014	0	0005	0033	0012	0	0	1	1	1	0		00
958	0014	0014	0014	0	0005	0033	0005	0	0	0	1	1	0		01
959	0014	0014	0014	0	0005	0033	0002	0	0	0	1	1	0		10
960	0014	0014	0014	0	0005	0033	0011	0	0	1	1	1	0		11
961	0014	0014	0014	0	0005	0033	0014	0	0	1	1	1	0		00
962	0014	0014	0014	0	0005	0033	0006	0	0	0	1	1	0		10
963	0014	0014	0014	0	0005	0033	0013	0	0	1	1	1	0		11
964	0014	0014	0014	0	0005	0033	0015	0	0	1	1	1	0		11
965	0014	0014	0014	0	0005	0033	0016	0	0	1	1	1	0		10
966	0014	0014	0014	0	0005	0033	0017	0	1	1	0	0	0		01
967	0014	0014	0000	0	0003	0037	0000	0	0	0	1	1	1		
968	0014	0014	0014	0	0006	0034	0000	0	0	0	1	1	1		01
969	0014	0014	0014	0	0006	0034	0001	0	0	0	1	1	0		01
970	0014	0014	0014	0	0006	0034	0003	0	0	0	1	1	0		01
971	0014	0014	0014	0	0006	0034	0007	0	0	0	1	1	0		00
972	0014	0014	0014	0	0006	0034	0016	0	0	1	1	1	0		10
973	0014	0014	0014	0	0006	0034	0014	0	0	1	1	1	0		10
974	0014	0014	0014	0	0006	0034	0010	0	0	1	1	1	0		10
975	0014	0014	0014	0	0006	0034	0000	0	0	0	1	1	1		01
976	0014	0014	0014	0	0006	0034	0001	0	0	0	1	1	0		00
977	0014	0014	0014	0	0006	0034	0002	0	0	0	1	1	0		01
978	0014	0014	0014	0	0006	0034	0005	0	0	0	1	1	0		00
979	0014	0014	0014	0	0006	0034	0012	0	0	1	1	1	0		10
980	0014	0014	0014	0	0006	0034	0004	0	0	0	1	1	0		01
981	0014	0014	0014	0	0006	0034	0011	0	0	1	1	1	0		11
982	0014	0014	0014	0	0006	0034	0003	0	0	0	1	1	0		00
983	0014	0014	0014	0	0006	0034	0006	0	0	0	1	1	0		01
984	0014	0014	0014	0	0006	0034	0015	0	0	1	1	1	0		11
985	0014	0014	0014	0	0006	0034	0013	0	0	1	1	1	0		11
986	0014	0014	0014	0	0006	0034	0007	0	0	0	1	1	0		01

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_{IN}	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
987	0014	0014	0014	0	0006	0034	0017	0	1	1	0	0	0		10
988	0014	0014	0000	0	0003	0037	0000	0	0	0	1	1	1		
989	0014	0014	0014	0	0007	0033	0000	0	0	0	1	1	1		01
990	0014	0014	0014	0	0007	0033	0001	0	0	0	1	1	0		01
991	0014	0014	0014	0	0007	0033	0003	0	0	0	1	1	0		01
992	0014	0014	0014	0	0007	0033	0007	0	0	0	1	1	0		00
993	0014	0014	0014	0	0007	0033	0016	0	0	1	1	1	0		10
994	0014	0014	0014	0	0007	0033	0014	0	0	1	1	1	0		10
995	0014	0014	0014	0	0007	0033	0010	0	0	1	1	1	0		10
996	0014	0014	0014	0	0007	0033	0000	0	0	0	1	1	1		01
997	0014	0014	0014	0	0007	0033	0001	0	0	0	1	1	0		00
998	0014	0014	0014	0	0007	0033	0002	0	0	0	1	1	0		01
999	0014	0014	0014	0	0007	0033	0005	0	0	0	1	1	0		00
1000	0014	0014	0014	0	0007	0033	0012	0	0	1	1	1	0		10
1001	0014	0014	0014	0	0007	0033	0004	0	0	0	1	1	0		01
1002	0014	0014	0014	0	0007	0033	0011	0	0	1	1	1	0		11
1003	0014	0014	0014	0	0007	0033	0003	0	0	0	1	1	0		00
1004	0014	0014	0014	0	0007	0033	0006	0	0	0	1	1	0		01
1005	0014	0014	0014	0	0007	0033	0015	0	0	1	1	1	0		11
1006	0014	0014	0014	0	0007	0033	0013	0	0	1	1	1	0		11
1007	0014	0014	0014	0	0007	0033	0007	0	0	0	1	1	0		01
1008	0014	0014	0014	0	0007	0033	0017	0	1	1	0	0	0		10
1009	0015	0015	0000	0	0003	0037	0000	0	0	0	1	1	1		
1010	0015	0015	0015	0	0004	0034	0000	0	0	0	1	1	1		10
1011	0015	0015	0015	0	0004	0034	0010	0	0	1	1	1	0		10
1012	0015	0015	0015	0	0004	0034	0014	0	0	1	1	1	0		10
1013	0015	0015	0015	0	0004	0034	0016	0	0	1	1	1	0		00
1014	0015	0015	0015	0	0004	0034	0007	0	0	0	1	1	0		01
1015	0015	0015	0015	0	0004	0034	0003	0	0	0	1	1	0		01
1016	0015	0015	0015	0	0004	0034	0001	0	0	0	1	1	0		01
1017	0015	0015	0015	0	0004	0034	0000	0	0	0	1	1	1		10
1018	0015	0015	0015	0	0004	0034	0010	0	0	1	1	1	0		00
1019	0015	0015	0015	0	0004	0034	0004	0	0	0	1	1	0		10
1020	0015	0015	0015	0	0004	0034	0012	0	0	1	1	1	0		00

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
1021	0015	0015	0015	0	0004	0034	0005	0	0	0	1	1	0		01
1022	0015	0015	0015	0	0004	0034	0002	0	0	0	1	1	0		10
1023	0015	0015	0015	0	0004	0034	0011	0	0	1	1	1	0		11
1024	0015	0015	0015	0	0004	0034	0014	0	0	1	1	1	0		00
1025	0015	0015	0015	0	0004	0034	0006	0	0	0	1	1	0		10
1026	0015	0015	0015	0	0004	0034	0013	0	0	1	1	1	0		11
1027	0015	0015	0015	0	0004	0034	0015	0	0	1	1	1	0		11
1028	0015	0015	0015	0	0004	0034	0016	0	0	1	1	1	0		10
1029	0015	0015	0015	0	0004	0034	0017	0	**1**	1	**0**	**0**	0		01
1030	0015	0015	0000	0	0003	0037	0000	0	0	0	1	1	**1**		
1031	0015	0015	0015	0	0005	0033	0000	0	0	0	1	1	1		10
1032	0015	0015	0015	0	0005	0033	0010	0	0	1	1	1	0		10
1033	0015	0015	0015	0	0005	0033	0014	0	0	1	1	1	0		10
1034	0015	0015	0015	0	0005	0033	0016	0	0	1	1	1	0		00
1035	0015	0015	0015	0	0005	0033	0007	0	0	0	1	1	0		01
1036	0015	0015	0015	0	0005	0033	0003	0	0	0	1	1	0		01
1037	0015	0015	0015	0	0005	0033	0001	0	0	0	1	1	0		01
1038	0015	0015	0015	0	0005	0033	0000	0	0	0	1	1	**1**		10
1039	0015	0015	0015	0	0005	0033	0010	0	0	1	1	1	0		00
1040	0015	0015	0015	0	0005	0033	0004	0	0	0	1	1	0		10
1041	0015	0015	0015	0	0005	0033	0012	0	0	1	1	1	0		00
1042	0015	0015	0015	0	0005	0033	0005	0	0	0	1	1	0		01
1043	0015	0015	0015	0	0005	0033	0002	0	0	0	1	1	0		10
1044	0015	0015	0015	0	0005	0033	0011	0	0	1	1	1	0		11
1045	0015	0015	0015	0	0005	0033	0014	0	0	1	1	1	0		00
1046	0015	0015	0015	0	0005	0033	0006	0	0	0	1	1	0		10
1047	0015	0015	0015	0	0005	0033	0013	0	0	1	1	1	0		11
1048	0015	0015	0015	0	0005	0033	0015	0	0	1	1	1	0		11
1049	0015	0015	0015	0	0005	0033	0016	0	0	1	1	1	0		10
1050	0015	0015	0015	0	0005	0033	0017	0	**1**	1	**0**	**0**	0		01
1051	0015	0015	0000	0	0003	0037	0000	0	0	0	1	1	**1**		
1052	0015	0015	0015	0	0006	0034	0000	0	0	0	1	1	**1**		01
1053	0015	0015	0015	0	0006	0034	0001	0	0	0	1	1	0		01
1054	0015	0015	0015	0	0006	0034	0003	0	0	0	1	1	0		01

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
1055	0015	0015	0015	0	0006	0034	0007	0	0	0	1	1	0		00
1056	0015	0015	0015	0	0006	0034	0016	0	0	1	1	1	0		10
1057	0015	0015	0015	0	0006	0034	0014	0	0	1	1	1	0		10
1058	0015	0015	0015	0	0006	0034	0010	0	0	1	1	1	0		10
1059	0015	0015	0015	0	0006	0034	0000	0	0	0	1	1	1		01
1060	0015	0015	0015	0	0006	0034	0001	0	0	0	1	1	0		00
1061	0015	0015	0015	0	0006	0034	0002	0	0	0	1	1	0		01
1062	0015	0015	0015	0	0006	0034	0005	0	0	0	1	1	0		00
1063	0015	0015	0015	0	0006	0034	0012	0	0	1	1	1	0		10
1064	0015	0015	0015	0	0006	0034	0004	0	0	0	1	1	0		01
1065	0015	0015	0015	0	0006	0034	0011	0	0	1	1	1	0		11
1066	0015	0015	0015	0	0006	0034	0003	0	0	0	1	1	0		00
1067	0015	0015	0015	0	0006	0034	0006	0	0	0	1	1	0		01
1068	0015	0015	0015	0	0006	0034	0015	0	0	1	1	1	0		11
1069	0015	0015	0015	0	0006	0034	0013	0	0	1	1	1	0		11
1070	0015	0015	0015	0	0006	0034	0007	0	0	0	1	1	0		01
1071	0015	0015	0015	0	0006	0034	0017	0	1	1	0	0	0		10
1072	0015	0015	0000	0	0003	0037	0000	0	0	0	1	1	1		
1073	0015	0015	0015	0	0007	0033	0000	0	0	0	1	1	1		01
1074	0015	0015	0015	0	0007	0033	0001	0	0	0	1	1	0		01
1075	0015	0015	0015	0	0007	0033	0003	0	0	0	1	1	0		01
1076	0015	0015	0015	0	0007	0033	0007	0	0	0	1	1	0		00
1077	0015	0015	0015	0	0007	0033	0016	0	0	1	1	1	0		10
1078	0015	0015	0015	0	0007	0033	0014	0	0	1	1	1	0		10
1079	0015	0015	0015	0	0007	0033	0010	0	0	1	1	1	0		10
1080	0015	0015	0015	0	0007	0033	0000	0	0	0	1	1	1		01
1081	0015	0015	0015	0	0007	0033	0001	0	0	0	1	1	0		00
1082	0015	0015	0015	0	0007	0033	0002	0	0	0	1	1	0		01
1083	0015	0015	0015	0	0007	0033	0005	0	0	0	1	1	0		00
1084	0015	0015	0015	0	0007	0033	0012	0	0	1	1	1	0		10
1085	0015	0015	0015	0	0007	0033	0004	0	0	0	1	1	0		01
1086	0015	0015	0015	0	0007	0033	0011	0	0	1	1	1	0		11
1087	0015	0015	0015	0	0007	0033	0003	0	0	0	1	1	0		00
1088	0015	0015	0015	0	0007	0033	0006	0	0	0	1	1	0		01

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
1089	0015	0015	0015	0	0007	0033	0015	0	0	1	1	1	0		11
1090	0015	0015	0015	0	0007	0033	0013	0	0	1	1	1	0		11
1091	0015	0015	0015	0	0007	0033	0007	0	0	0	1	1	0		01
1092	0015	0015	0015	0	0007	0033	0017	0	1	1	0	0	0		10
1093	0016	0016	0000	0	0003	0037	0000	0	0	0	1	1	1		
1094	0016	0016	0016	0	0004	0034	0000	0	0	0	1	1	1		10
1095	0016	0016	0016	0	0004	0034	0010	0	0	1	1	1	0		10
1096	0016	0016	0016	0	0004	0034	0014	0	0	1	1	1	0		10
1097	0016	0016	0016	0	0004	0034	0016	0	0	1	1	1	0		00
1098	0016	0016	0016	0	0004	0034	0007	0	0	0	1	1	0		01
1099	0016	0016	0016	0	0004	0034	0003	0	0	0	1	1	0		01
1100	0016	0016	0016	0	0004	0034	0001	0	0	0	1	1	0		01
1101	0016	0016	0016	0	0004	0034	0000	0	0	0	1	1	1		10
1102	0016	0016	0016	0	0004	0034	0010	0	0	1	1	1	0		00
1103	0016	0016	0016	0	0004	0034	0004	0	0	0	1	1	0		10
1104	0016	0016	0016	0	0004	0034	0012	0	0	1	1	1	0		00
1105	0016	0016	0016	0	0004	0034	0005	0	0	0	1	1	0		01
1106	0016	0016	0016	0	0004	0034	0002	0	0	0	1	1	0		10
1107	0016	0016	0016	0	0004	0034	0011	0	0	1	1	1	0		11
1108	0016	0016	0016	0	0004	0034	0014	0	0	1	1	1	0		00
1109	0016	0016	0016	0	0004	0034	0006	0	0	0	1	1	0		10
1110	0016	0016	0016	0	0004	0034	0013	0	0	1	1	1	0		11
1111	0016	0016	0016	0	0004	0034	0015	0	0	1	1	1	0		11
1112	0016	0016	0016	0	0004	0034	0016	0	0	1	1	1	0		10
1113	0016	0016	0016	0	0004	0034	0017	0	1	1	0	0	0		01
1114	0016	0016	0000	0	0003	0037	0000	0	0	0	1	1	1		
1115	0016	0016	0016	0	0005	0033	0000	0	0	0	1	1	1		10
1116	0016	0016	0016	0	0005	0033	0010	0	0	1	1	1	0		10
1117	0016	0016	0016	0	0005	0033	0014	0	0	1	1	1	0		10
1118	0016	0016	0016	0	0005	0033	0016	0	0	1	1	1	0		00
1119	0016	0016	0016	0	0005	0033	0007	0	0	0	1	1	0		01
1120	0016	0016	0016	0	0005	0033	0003	0	0	0	1	1	0		01
1121	0016	0016	0016	0	0005	0033	0001	0	0	0	1	1	0		01
1122	0016	0016	0016	0	0005	0033	0000	0	0	0	1	1	1		10

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
1123	0016	0016	0016	0	0005	0033	0010	0	0	1	1	1	0		00
1124	0016	0016	0016	0	0005	0033	0004	0	0	0	1	1	0		10
1125	0016	0016	0016	0	0005	0033	0012	0	0	1	1	1	0		00
1126	0016	0016	0016	0	0005	0033	0005	0	0	0	1	1	0		01
1127	0016	0016	0016	0	0005	0033	0002	0	0	0	1	1	0		10
1128	0016	0016	0016	0	0005	0033	0011	0	0	1	1	1	0		11
1129	0016	0016	0016	0	0005	0033	0014	0	0	1	1	1	0		00
1130	0016	0016	0016	0	0005	0033	0006	0	0	0	1	1	0		10
1131	0016	0016	0016	0	0005	0033	0013	0	0	1	1	1	0		11
1132	0016	0016	0016	0	0005	0033	0015	0	0	1	1	1	0		11
1133	0016	0016	0016	0	0005	0033	0016	0	0	1	1	1	0		10
1134	0016	0016	0016	0	0005	0033	0017	0	1	1	0	0	0		01
1135	0016	0016	0000	0	0003	0037	0000	0	0	0	1	1	1		
1136	0016	0016	0016	0	0006	0034	0000	0	0	0	1	1	1		01
1137	0016	0016	0016	0	0006	0034	0001	0	0	0	1	1	0		01
1138	0016	0016	0016	0	0006	0034	0003	0	0	0	1	1	0		01
1139	0016	0016	0016	0	0006	0034	0007	0	0	0	1	1	0		00
1140	0016	0016	0016	0	0006	0034	0016	0	0	1	1	1	0		10
1141	0016	0016	0016	0	0006	0034	0014	0	0	1	1	1	0		10
1142	0016	0016	0016	0	0006	0034	0010	0	0	1	1	1	0		10
1143	0016	0016	0016	0	0006	0034	0000	0	0	0	1	1	1		01
1144	0016	0016	0016	0	0006	0034	0001	0	0	0	1	1	0		00
1145	0016	0016	0016	0	0006	0034	0002	0	0	0	1	1	0		01
1146	0016	0016	0016	0	0006	0034	0005	0	0	0	1	1	0		00
1147	0016	0016	0016	0	0006	0034	0012	0	0	1	1	1	0		10
1148	0016	0016	0016	0	0006	0034	0004	0	0	0	1	1	0		01
1149	0016	0016	0016	0	0006	0034	0011	0	0	1	1	1	0		11
1150	0016	0016	0016	0	0006	0034	0003	0	0	0	1	1	0		00
1151	0016	0016	0016	0	0006	0034	0006	0	0	0	1	1	0		01
1152	0016	0016	0016	0	0006	0034	0015	0	0	1	1	1	0		11
1153	0016	0016	0016	0	0006	0034	0013	0	0	1	1	1	0		11
1154	0016	0016	0016	0	0006	0034	0007	0	0	0	1	1	0		01
1155	0016	0016	0016	0	0006	0034	0017	0	1	1	0	0	0		10
1156	0016	0016	0000	0	0003	0037	0000	0	0	0	1	1	1		

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
1157	0016	0016	0016	0	0007	0033	0000	0	0	0	1	1	1		01
1158	0016	0016	0016	0	0007	0033	0001	0	0	0	1	1	0		01
1159	0016	0016	0016	0	0007	0033	0003	0	0	0	1	1	0		01
1160	0016	0016	0016	0	0007	0033	0007	0	0	0	1	1	0		00
1161	0016	0016	0016	0	0007	0033	0016	0	0	1	1	1	0		10
1162	0016	0016	0016	0	0007	0033	0014	0	0	1	1	1	0		10
1163	0016	0016	0016	0	0007	0033	0010	0	0	1	1	1	0		10
1164	0016	0016	0016	0	0007	0033	0000	0	0	0	1	1	1		01
1165	0016	0016	0016	0	0007	0033	0001	0	0	0	1	1	0		00
1166	0016	0016	0016	0	0007	0033	0002	0	0	0	1	1	0		01
1167	0016	0016	0016	0	0007	0033	0005	0	0	0	1	1	0		00
1168	0016	0016	0016	0	0007	0033	0012	0	0	1	1	1	0		10
1169	0016	0016	0016	0	0007	0033	0004	0	0	0	1	1	0		01
1170	0016	0016	0016	0	0007	0033	0011	0	0	1	1	1	0		11
1171	0016	0016	0016	0	0007	0033	0003	0	0	0	1	1	0		00
1172	0016	0016	0016	0	0007	0033	0006	0	0	0	1	1	0		01
1173	0016	0016	0016	0	0007	0033	0015	0	0	1	1	1	0		11
1174	0016	0016	0016	0	0007	0033	0013	0	0	1	1	1	0		11
1175	0016	0016	0016	0	0007	0033	0007	0	0	0	1	1	0		01
1176	0016	0016	0016	0	0007	0033	0017	0	1	1	0	0	0		10
1177	0017	0017	0000	0	0003	0037	0000	0	0	0	1	1	1		
1178	0017	0017	0017	0	0004	0034	0000	0	0	0	1	1	1		10
1179	0017	0017	0017	0	0004	0034	0010	0	0	1	1	1	0		10
1180	0017	0017	0017	0	0004	0034	0014	0	0	1	1	1	0		10
1181	0017	0017	0017	0	0004	0034	0016	0	0	1	1	1	0		00
1182	0017	0017	0017	0	0004	0034	0007	0	0	0	1	1	0		01
1183	0017	0017	0017	0	0004	0034	0003	0	0	0	1	1	0		01
1184	0017	0017	0017	0	0004	0034	0001	0	0	0	1	1	0		01
1185	0017	0017	0017	0	0004	0034	0000	0	0	0	1	1	1		10
1186	0017	0017	0017	0	0004	0034	0010	0	0	1	1	1	0		00
1187	0017	0017	0017	0	0004	0034	0004	0	0	0	1	1	0		10
1188	0017	0017	0017	0	0004	0034	0012	0	0	1	1	1	0		00
1189	0017	0017	0017	0	0004	0034	0005	0	0	0	1	1	0		01
1190	0017	0017	0017	0	0004	0034	0002	0	0	0	1	1	0		10

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
1191	0017	0017	0017	0	0004	0034	0011	0	0	1	1	1	0		11
1192	0017	0017	0017	0	0004	0034	0014	0	0	1	1	1	0		00
1193	0017	0017	0017	0	0004	0034	0006	0	0	0	1	1	0		10
1194	0017	0017	0017	0	0004	0034	0013	0	0	1	1	1	0		11
1195	0017	0017	0017	0	0004	0034	0015	0	0	1	1	1	0		11
1196	0017	0017	0017	0	0004	0034	0016	0	0	1	1	1	0		10
1197	0017	0017	0017	0	0004	0034	0017	0	1	1	0	0	0		01
1198	0017	0017	0000	0	0003	0037	0000	0	0	0	1	1	1		
1199	0017	0017	0017	0	0005	0033	0000	0	0	0	1	1	1		10
1200	0017	0017	0017	0	0005	0033	0010	0	0	1	1	1	0		10
1201	0017	0017	0017	0	0005	0033	0014	0	0	1	1	1	0		10
1202	0017	0017	0017	0	0005	0033	0016	0	0	1	1	1	0		00
1203	0017	0017	0017	0	0005	0033	0007	0	0	0	1	1	0		01
1204	0017	0017	0017	0	0005	0033	0003	0	0	0	1	1	0		01
1205	0017	0017	0017	0	0005	0033	0001	0	0	0	1	1	0		01
1206	0017	0017	0017	0	0005	0033	0000	0	0	0	1	1	1		10
1207	0017	0017	0017	0	0005	0033	0010	0	0	1	1	1	0		00
1208	0017	0017	0017	0	0005	0033	0004	0	0	0	1	1	0		10
1209	0017	0017	0017	0	0005	0033	0012	0	0	1	1	1	0		00
1210	0017	0017	0017	0	0005	0033	0005	0	0	0	1	1	0		01
1211	0017	0017	0017	0	0005	0033	0002	0	0	0	1	1	0		10
1212	0017	0017	0017	0	0005	0033	0011	0	0	1	1	1	0		11
1213	0017	0017	0017	0	0005	0033	0014	0	0	1	1	1	0		00
1214	0017	0017	0017	0	0005	0033	0006	0	0	0	1	1	0		10
1215	0017	0017	0017	0	0005	0033	0013	0	0	1	1	1	0		11
1216	0017	0017	0017	0	0005	0033	0015	0	0	1	1	1	0		11
1217	0017	0017	0017	0	0005	0033	0016	0	0	1	1	1	0		10
1218	0017	0017	0017	0	0005	0033	0017	0	1	1	0	0	0		01
1219	0017	0017	0000	0	0003	0037	0000	0	0	0	1	1	1		
1220	0017	0017	0017	0	0006	0034	0000	0	0	0	1	1	1		01
1221	0017	0017	0017	0	0006	0034	0001	0	0	0	1	1	0		01
1222	0017	0017	0017	0	0006	0034	0003	0	0	0	1	1	0		01
1223	0017	0017	0017	0	0006	0034	0007	0	0	0	1	1	0		00
1224	0017	0017	0017	0	0006	0034	0016	0	0	1	1	1	0		10

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
1225	0017	0017	0017	0	0006	0034	0014	0	0	1	1	1	0		10
1226	0017	0017	0017	0	0006	0034	0010	0	0	1	1	1	0		10
1227	0017	0017	0017	0	0006	0034	0000	0	0	0	1	1	1		01
1228	0017	0017	0017	0	0006	0034	0001	0	0	0	1	1	0		00
1229	0017	0017	0017	0	0006	0034	0002	0	0	0	1	1	0		01
1230	0017	0017	0017	0	0006	0034	0005	0	0	0	1	1	0		00
1231	0017	0017	0017	0	0006	0034	0012	0	0	1	1	1	0		10
1232	0017	0017	0017	0	0006	0034	0004	0	0	0	1	1	0		01
1233	0017	0017	0017	0	0006	0034	0011	0	0	1	1	1	0		11
1234	0017	0017	0017	0	0006	0034	0003	0	0	0	1	1	0		00
1235	0017	0017	0017	0	0006	0034	0006	0	0	0	1	1	0		01
1236	0017	0017	0017	0	0006	0034	0015	0	0	1	1	1	0		11
1237	0017	0017	0017	0	0006	0034	0013	0	0	1	1	1	0		11
1238	0017	0017	0017	0	0006	0034	0007	0	0	0	1	1	0		01
1239	0017	0017	0017	0	0006	0034	0017	0	1	1	0	0	0		10
1240	0017	0017	0000	0	0003	0037	0000	0	0	0	1	1	1		
1241	0017	0017	0017	0	0007	0033	0000	0	0	0	1	1	1		01
1242	0017	0017	0017	0	0007	0033	0001	0	0	0	1	1	0		01
1243	0017	0017	0017	0	0007	0033	0003	0	0	0	1	1	0		01
1244	0017	0017	0017	0	0007	0033	0007	0	0	0	1	1	0		00
1245	0017	0017	0017	0	0007	0033	0016	0	0	1	1	1	0		10
1246	0017	0017	0017	0	0007	0033	0014	0	0	1	1	1	0		10
1247	0017	0017	0017	0	0007	0033	0010	0	0	1	1	1	0		10
1248	0017	0017	0017	0	0007	0033	0000	0	0	0	1	1	1		01
1249	0017	0017	0017	0	0007	0033	0001	0	0	0	1	1	0		00
1250	0017	0017	0017	0	0007	0033	0002	0	0	0	1	1	0		01
1251	0017	0017	0017	0	0007	0033	0005	0	0	0	1	1	0		00
1252	0017	0017	0017	0	0007	0033	0012	0	0	1	1	1	0		10
1253	0017	0017	0017	0	0007	0033	0004	0	0	0	1	1	0		01
1254	0017	0017	0017	0	0007	0033	0011	0	0	1	1	1	0		11
1255	0017	0017	0017	0	0007	0033	0003	0	0	0	1	1	0		00
1256	0017	0017	0017	0	0007	0033	0006	0	0	0	1	1	0		01
1257	0017	0017	0017	0	0007	0033	0015	0	0	1	1	1	0		11
1258	0017	0017	0017	0	0007	0033	0013	0	0	1	1	1	0		11

SET 3

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
1259	0017	0017	0017	0	0007	0033	0007	0	0	0	1	1	0		01
1260	0017	0017	0017	0	0007	0033	0017	0	1	1	0	0	0		10

SET 4

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
1	0000	0000	0000	0	0003	0037	0000	0	0	0	1	1	1		
2	0001	0001	0000	0	0003	0037	0000	0	0	0	1	1	1		
3	0002	0002	0000	0	0003	0037	0000	0	0	0	1	1	1		
4	0003	0003	0000	0	0003	0037	0000	0	0	0	1	1	1		
5	0004	0004	0000	0	0003	0037	0000	0	0	0	1	1	1		
6	0005	0005	0000	0	0003	0037	0000	0	0	0	1	1	1		
7	0006	0006	0000	0	0003	0037	0000	0	0	0	1	1	1		
8	0007	0007	0000	0	0003	0037	0000	0	0	0	1	1	1		
9	0010	0010	0000	0	0003	0037	0000	0	0	0	1	1	1		
10	0011	0011	0000	0	0003	0037	0000	0	0	0	1	1	1		
11	0012	0012	0000	0	0003	0037	0000	0	0	0	1	1	1		
12	0013	0013	0000	0	0003	0037	0000	0	0	0	1	1	1		
13	0014	0014	0000	0	0003	0037	0000	0	0	0	1	1	1		
14	0015	0015	0000	0	0003	0037	0000	0	0	0	1	1	1		
15	0016	0016	0000	0	0003	0037	0000	0	0	0	1	1	1		
16	0017	0017	0000	0	0003	0037	0000	0	0	0	1	1	1		
17	0000	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
18	0001	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
19	0002	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
20	0003	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
21	0004	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
22	0005	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
23	0006	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
24	0007	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
25	0010	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
26	0011	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
27	0012	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
28	0013	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
29	0014	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
30	0015	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
31	0016	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
32	0017	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
33	0000	0000	0000	0	0001	0034	0000	0	0	0	1	1	1		
34	0000	0000	0000	0	0003	0024	0017	0	1	1	0	0	0		

SET 4

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
35	00 01	0001	0000	0	0001	0034	00 00	0	0	0	1	1	1		
36	00 01	0001	00 00	0	0003	0024	0017	0	1	1	0	0	0		
37	00 02	0002	00 00	0	0001	0034	00 00	0	0	0	1	1	1		
38	00 02	0002	00 00	0	0003	0024	0017	0	1	1	0	0	0		
39	00 03	0003	00 00	0	0001	0034	00 00	0	0	0	1	1	1		
40	00 03	0003	00 00	0	0003	0024	0017	0	1	1	0	0	0		
41	00 04	0004	00 00	0	0001	0034	00 00	0	0	0	1	1	1		
42	00 04	0004	00 00	0	0003	0024	0017	0	1	1	0	0	0		
43	00 05	0005	00 00	0	0001	0034	00 00	0	0	0	1	1	1		
44	00 05	0005	00 00	0	0003	0024	0017	0	1	1	0	0	0		
45	00 06	0006	00 00	0	0001	0034	00 00	0	0	1	1	1	1		
46	00 06	0006	00 00	0	0003	0024	0017	0	1	1	0	0	0		
47	00 07	0007	00 00	0	0001	0034	00 00	0	0	0	1	1	1		
48	00 07	0007	00 00	0	0003	0024	0017	0	1	1	0	0	0		
49	00 10	0010	00 00	0	0001	0034	00 00	0	0	0	1	1	1		
50	00 10	0010	00 00	0	0003	0024	0017	0	1	1	0	0	0		
51	00 11	0011	00 00	0	0001	0034	00 00	0	0	0	1	1	1		
52	00 11	0011	00 00	0	0003	0024	0017	0	1	1	0	0	0		
53	00 12	0012	00 00	0	0001	0034	00 00	0	0	0	1	1	1		
54	00 12	0012	00 00	0	0003	0024	0017	0	1	1	0	0	0		
55	00 13	0013	00 00	0	0001	0034	00 00	0	0	0	1	1	1		
56	00 13	0013	00 00	0	0003	0024	0017	0	1	1	0	0	0		
57	00 14	0014	00 00	0	0001	0034	00 00	0	0	0	1	1	1		
58	00 14	0014	00 00	0	0003	0024	0017	0	1	1	0	0	0		
59	00 15	0015	00 00	0	0001	0034	00 00	0	0	0	1	1	1		
60	00 15	0015	00 00	0	0003	0024	0017	0	1	1	0	0	0		
61	00 16	0016	00 00	0	0001	0034	00 00	0	0	0	1	1	1		
62	00 16	0016	00 00	0	0003	0024	0017	0	1	1	0	0	0		
63	00 17	0017	00 00	0	0001	0034	00 00	0	0	0	1	1	1		
64	00 17	0017	00 00	0	0003	0024	0017	0	1	1	0	0	0		
65	00 17	0017	00 00	0	0001	0034	0017	0	1	1	0	0	0		
66	00 17	0017	00 00	0	0003	0024	00 00	0	0	0	1	1	1		
67	00 16	0016	00 00	0	0001	0034	0017	0	1	1	1	0	0		
68	00 16	0016	00 00	0	0003	0024	00 00	0	0	0	1	1	1		

SET 4

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
69	0015	0015	0000	0	0001	0034	0017	0	1	1	0	0	0		
70	0015	0015	0000	0	0003	0024	0000	0	0	0	1	1	1		
71	0014	0014	0000	0	0001	0034	0017	0	1	1	0	0	0		
72	0014	0014	0000	0	0003	0024	0000	0	0	0	1	1	1		
73	0013	0013	0000	0	0001	0034	0017	0	1	1	0	0	0		
74	0013	0013	0000	0	0003	0024	0000	0	0	0	1	1	1		
75	0012	0012	0000	0	0001	0034	0017	0	1	1	0	0	0		
76	0012	0012	0000	0	0003	0024	0000	0	0	0	1	1	1		
77	0011	0011	0000	0	0001	0034	0017	0	1	1	0	0	0		
78	0011	0011	0000	0	0003	0024	0000	0	0	0	1	1	1		
79	0010	0010	0000	0	0001	0034	0017	0	1	1	0	0	0		
80	0010	0010	0000	0	0003	0024	0000	0	0	0	1	1	1		
81	0007	0007	0000	0	0001	0034	0017	0	1	1	0	0	0		
82	0007	0007	0000	0	0003	0024	0000	0	0	0	1	1	1		
83	0006	0006	0000	0	0001	0034	0017	0	1	1	0	0	0		
84	0006	0006	0000	0	0003	0024	0000	0	0	0	1	1	1		
85	0005	0005	0000	0	0001	0034	0017	0	1	1	0	0	0		
86	0005	0005	0000	0	0003	0024	0000	0	0	0	1	1	1		
87	0004	0004	0000	0	0001	0034	0017	0	1	1	0	0	0		
88	0004	0004	0000	0	0003	0024	0000	0	0	0	1	1	1		
89	0003	0003	0000	0	0001	0034	0017	0	1	1	0		0		
90	0003	0003	0000	0	0003	0024	0000	0	0	0	1	1	1		
91	0002	0002	0000	0	0001	0034	0017	0	1	1	0	0	0		
92	0002	0002	0000	0	0003	0024	0000	0	0	0	1	1	1		
93	0001	0001	0000	0	0001	0034	0017	0	1	1	0	0	0		
94	0001	0001	0000	0	0003	0024	0000	0	0	0	1	1	1		
95	0000	0000	0000	0	0001	0034	0017	0	1	1	0	0	0		
96	0000	0000	0000	0	0003	0024	0000	0	0	0	1	1	1		
97	0000	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
98	0001	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
99	0002	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
100	0003	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
101	0004	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		
102	0005	0000	0017	0	0001	0034	0000	0	0	0	1	1	1		

SET 4

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
103	00 06	0000	00 17	0	0001	0034	00 00	0	0	0	1	1	1		
104	00 07	0000	00 17	0	0001	0034	00 00	0	0	0	1	1	1		
105	00 10	0000	00 17	0	0001	0034	00 00	0	0	0	1	1	1		
106	00 11	0000	00 17	0	0001	0034	00 00	0	0	0	1	1	1		
107	00 12	0000	00 17	0	0001	0034	00 00	0	0	0	1	1	1		
108	00 13	0000	00 17	0	0001	0034	00 00	0	0	0	1	1	1		
109	00 14	0000	00 17	0	0001	0034	00 00	0	0	0	1	1	1		
110	00 15	0000	00 17	0	0001	0034	00 00	0	0	0	1	1	1		
111	00 16	0000	00 17	0	0001	0034	00 00	0	0	0	1	1	1		
112	00 17	0000	00 17	0	0001	0034	00 00	0	0	0	1	1	1		
113	00 00	0000	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
114	00 00	0001	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
115	00 00	0002	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
116	00 00	0003	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
117	00 00	0004	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
118	00 00	0005	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
119	00 00	0006	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
120	00 00	0007	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
121	00 00	0000	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
122	00 00	0001	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
123	00 00	0002	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
124	00 00	0003	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
125	00 00	0004	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
126	00 00	0005	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
127	00 00	0006	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
128	00 00	0007	00 17	0	0003	0037	00 17	0	1	1	0	0	0		
129	00 00	0000	00 00	0	0001	0033	00 17	0	1	1	0	0	0		
130	00 00	0001	00 00	0	0001	0033	00 17	0	1	1	0	0	0		
131	00 00	0002	00 00	0	0001	0033	00 17	0	1	1	0	0	0		
132	00 00	0003	00 00	0	0001	0033	00 17	0	1	1	0	0	0		
133	00 00	0004	00 00	0	0001	0033	00 17	0	1	1	0	0	0		
134	00 00	0005	00 00	0	0001	0033	00 17	0	1	1	0	0	0		
135	00 00	0006	00 00	0	0001	0033	00 17	0	1	1	0	0	0		
136	00 00	0007	00 00	0	0001	0033	00 17	0	1	1	0	0	0		

SET 4

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
137	0000	0010	0000	0	0001	0033	0017	0	1	1	0	0	0		
138	0000	0011	0000	0	0001	0033	0017	0	1	1	0	0	0		
139	0000	0012	0000	0	0001	0033	0017	0	1	1	0	0	0		
140	0000	0013	0000	0	0001	0033	0017	0	1	1	0	0	0		
141	0000	0014	0000	0	0001	0033	0017	0	1	1	0	0	0		
142	0000	0015	0000	0	0001	0033	0017	0	1	1	0	0	0		
143	0000	0016	0000	0	0001	0033	0017	0	1	1	0	0	0		
144	0000	0017	0000	0	0001	0033	0017	0	1	1	0	0	0		
145	0000	0000	0000	0	0001	0033	0017	0	1	1	0	0	0		
146	0000	0000	0000	0	0003	0023	0000	0	0	0	1	1	1		
147	0000	0001	0000	0	0001	0033	0017	0	1	1	0	0	0		
148	0000	0001	0000	0	0003	0023	0000	0	0	0	1	1	1		
149	0000	0002	0000	0	0001	0033	0017	0	1	1	0	0	0		
150	0000	0002	0000	0	0003	0023	0000	0	0	0	1	1	1		
151	0000	0003	0000	0	0001	0033	0017	0	1	1	0	0	0		
152	0000	0003	0000	0	0003	0023	0000	0	0	0	1	1	1		
153	0000	0004	0000	0	0001	0033	0017	0	1	1	0	0	0		
154	0000	0004	0000	0	0003	0023	0000	0	0	0	1	1	1		
155	0000	0005	0000	0	0001	0033	0017	0	1	1	0	0	0		
156	0000	0005	0000	0	0003	0023	0000	0	0	0	1	1	1		
157	0000	0006	0000	0	0001	0033	0017	0	1	1	0	0	0		
158	0000	0006	0000	0	0003	0023	0000	0	0	0	1	1	1		
159	0000	0007	0000	0	0001	0033	0017	0	1	1	0	0	0		
160	0000	0007	0000	0	0003	0023	0000	0	0	0	1	1	1		
161	0000	0010	0000	0	0001	0033	0017	0	1	1	0	0	0		
162	0000	0010	0000	0	0003	0023	0000	0	0	0	1	1	1		
163	0000	0011	0000	0	0001	0033	0017	0	1	1	0	0	0		
164	0000	0011	0000	0	0003	0023	0000	0	0	0	1	1	1		
165	0000	0012	0000	0	0001	0033	0017	0	1	1	0	0	0		
166	0000	0012	0000	0	0003	0023	0000	0	0	0	1	1	1		
167	0000	0013	0000	0	0001	0033	0017	0	1	1	0	0	0		
168	0000	0013	0000	0	0003	0033	0000	0	0	0	1	1	1		
169	0000	0014	0000	0	0001	0033	0017	0	1	1	0	1	0		
170	0000	0014	0000	0	0003	0023	0000	0	0	0	1	1	1		

SET 4

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
171	0000	00 15	0000	0	0001	0033	0017	0	1	1	0	0	0		
172	0000	00 15	0000	0	0003	0023	0000	0	0	0	1	1	1		
173	0000	00 16	0000	0	0001	0033	0017	0	1	1	0	0	0		
174	0000	00 16	0000	0	0003	0023	0000	0	0	0	1	1	1		
175	0000	00 17	0000	0	0001	0033	0017	0	1	1	0	0	0		
176	0000	00 17	0000	0	0003	0023	0000	0	0	0	1	1	1		
177	0000	00 17	0000	0	0001	0033	0000	0	0	0	1	1	1		
178	0000	00 17	0000	0	0003	0023	0017	0	1	1	0	0	0		
179	0000	00 16	0000	0	0001	0033	0000	0	0	0	1	1	1		
180	0000	00 16	0000	0	0003	0023	0017	0	1	1	0	0	0		
181	0000	00 15	0000	0	0001	0033	0000	0	0	0	1	1	1		
182	0000	00 15	0000	0	0003	0023	0017	0	1	1	0	0	0		
183	0000	00 14	0000	0	0001	0033	0000	0	0	0	1	1	1		
184	0000	00 14	0000	0	0003	0023	0017	0	1	1	0	0	0		
185	0000	00 13	0000	0	0001	0033	0000	0	0	0	1	1	1		
186	0000	00 13	0000	0	0003	0023	0017	0	1	1	0	0	0		
187	0000	00 12	0000	0	0001	0033	0000	0	0	0	1	1	1		
188	0000	00 12	0000	0	0003	0023	0017	0	1	1	0	0	0		
189	0000	00 11	0000	0	0001	0033	0000	0	0	0	1	1	1		
190	0000	00 11	0000	0	0003	0023	0017	0	1	1	0	0	0		
191	0000	00 10	0000	0	0001	0033	0000	0	0	0	1	1	1		
192	0000	00 10	0000	0	0003	0023	0017	0	1	1	0	0	0		
193	0000	00 07	0000	0	0001	0033	0000	0	0	0	1	1	1		
194	0000	00 07	0000	0	0003	0023	0017	0	1	1	0	0	0		
195	0000	00 06	0000	0	0001	0033	0000	0	0	0	1	1	1		
196	0000	00 06	0000	0	0003	0023	0017	0	1	1	0	0	0		
197	0000	00 05	0000	0	0001	0033	0000	0	0	0	1	1	1		
198	0000	00 05	0000	0	0003	0023	0017	0	1	1	0	0	0		
199	0000	00 04	0000	0	0001	0033	0000	0	0	0	1	1	1		
200	0000	00 04	0000	0	0003	0023	0017	0	1	1	0	0	0		
201	0000	00 03	0000	0	0001	0033	0000	0	0	0	1	1	1		
202	0000	00 03	0000	0	0003	0023	0017	0	1	1	0	0	0		
203	0000	00 02	0000	0	0001	0033	0000	0	0	0	1	1	1		
204	0000	00 02	0000	0	0003	0023	0017	0	1	1	1	0	0		

SET 4

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
205	0000	00 01	0000	0	0001	00 33	00 00	0	0	0	1	1	1		
206	0000	00 01	0000	0	0003	00 23	00 17	0	1	1	0	0	0		
207	0000	00 00	0000	0	0001	00 33	00 00	0	0	0	1	1	1		
208	0000	00 00	0000	0	0003	00 23	00 17	0	1	1	0	0	0		
209	0000	00 00	0000	0	0001	00 33	00 17	0	1	1	1	1	0		
210	0000	00 01	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
211	0000	00 02	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
212	0000	00 03	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
213	0000	00 04	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
214	0000	00 05	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
215	0000	00 06	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
216	0000	00 07	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
217	0000	00 10	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
218	0000	00 11	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
219	0000	00 12	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
220	0000	00 13	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
221	0000	00 14	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
222	0000	00 15	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
223	0000	00 16	0000	0	0001	00 33	00 17	0	1	1	0	0	0		
224	0000	00 17	0000	0	0001	00 33	00 17	0	1	1	0	0	0		

Set 5

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	CP/OE	Y_{3-0}	P	G	F_3	CN4	OVR	F_0	Q_{30}	R_{30}
1	00 00	0000	0017	0	0000	003 7	10	00 17	0	1	1	0	0	0	XX	XX
2	00 00	0000	0017	0	0000	003 7	00	00 17	0	1	1	0	0	0	XX	XX
3	00 00	0000	0017	0	0000	003 7	10	00 17	0	1	1	0	0	0	XX	XX
4	00 00	0000	0017	0	0003	003 7	00	00 17	0	1	1	0	0	0	XX	XX
5	00 00	0001	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
6	00 00	0002	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
7	00 00	0003	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
8	00 00	0004	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
9	00 00	0005	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
10	00 00	0006	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
11	00 00	0007	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
12	00 00	0010	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
13	00 00	0011	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
14	00 00	0012	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
15	00 00	0013	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
16	00 00	0014	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
17	00 00	0015	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
18	00 00	0016	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
19	00 00	0017	0000	0	0003	003 7	00	00 00	0	0	0	1	1	1	XX	XX
20	00 00	0017	0000	0	0001	003 4	10	00 17	0	1	1	0	0	0	XX	XX
21	00 01	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX
22	00 02	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX
23	00 03	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX
24	00 04	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX
25	00 05	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX
26	00 06	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX
27	00 07	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX
28	00 10	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX
29	00 11	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX
30	00 12	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX
31	00 13	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX
32	00 14	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX
33	00 15	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX
34	00 16 –	0017	0000	0	0001	003 4	10	00 00	0	0	0	1	1	1	XX	XX

SET 5

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	$\frac{CP}{OE}$	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
35	0017	0017	0017	0	0001	0034	10	0000	0	0	0	1	1	1	XX	XX
36	0000	0000	0017	0	0002	0037	10	0017	0	1	1	0	0	0	XX	XX
37	0000	0000	0017	0	0002	0037	00	0017	0	1	1	0	0	0	XX	XX
38	0000	0000	0000	0	0002	0037	00	0017	0	0	0	1	1	1	XX	XX
39	0001	0001	0000	0	0002	0037	00	0017	0	0	0	1	1	1	XX	XX
40	0001	0001	0001	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
41	0002	0002	0001	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
42	0002	0002	0002	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
43	0003	0003	0002	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
44	0003	0003	0003	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
45	0004	0004	0003	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
46	0004	0004	0004	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
47	0005	0005	0004	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
48	0005	0005	0005	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
49	0006	0006	0005	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
50	0006	0006	0006	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
51	0007	0007	0006	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
52	0007	0007	0007	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
53	0010	0010	0007	0	0002	0037	00	0017	0	0	0	1	1	0	XX	XX
54	0010	0010	0010	0	0002	0037	00	0017	0	0	1	1	1	0	XX	XX
55	0011	0011	0010	0	0002	0037	00	0017	0	0	1	1	1	0	XX	XX
56	0011	0011	0011	0	0002	0037	00	0017	0	0	1	1	1	0	XX	XX
57	0012	0012	0011	0	0002	0037	00	0017	0	0	1	1	1	0	XX	XX
58	0012	0012	0012	0	0002	0037	00	0017	0	0	1	1	1	0	XX	XX
59	0013	0013	0012	0	0002	0037	00	0017	0	0	1	1	1	0	XX	XX
60	0013	0013	0013	0	0002	0037	00	0017	0	0	1	1	1	0	XX	XX
61	0014	0014	0013	0	0002	0037	00	0017	0	0	1	1	1	0	XX	XX
62	0014	0014	0014	0	0002	0037	00	0017	0	0	1	1	1	0	XX	XX
63	0015	0015	0014	0	0002	0037	00	0017	0	0	1	1	1	0	XX	XX
64	0015	0015	0015	0	0002	0037	00	0017	0	0	1	1	1	0	XX	XX
65	0016	0016	0015	0	0002	0037	00	0017	0	0	1	1	1	0	XX	XX
66	0016	0016	0016	0	0002	0037	00	0017	0	0	1	1	1	0	XX	XX
67	0017	0017	0016	0	0002	0037	00	0017	0	1	1	0	0	0	XX	XX
68	0017	0017	0017	0	0002	0037	10	0017	0	1	1	0	0	0	XX	XX

SET 5

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	$\frac{CP}{\overline{OE}}$	Y_{3-0}	P	G	F3	CN4	OVR	F0	Q_{30}	R_{30}
69	00 17	00 17	0017	0	0002	0037	10	00 17	0	1	1	0	0	0	XX	XX
70	00 00	00 17	0017	0	0003	0034	10	00 00	0	0	0	1	1	1	XX	XX
71	00 01	00 16	0016	0	0003	0034	10	00 01	0	0	0	1	1	0	XX	XX
72	00 02	00 15	0015	0	0003	0034	10	00 02	0	0	0	1	1	0	XX	XX
73	00 03	00 14	0014	0	0003	0034	10	00 03	0	0	0	1	1	0	XX	XX
74	00 04	00 13	0013	0	0003	0034	10	00 04	0	0	0	1	1	0	XX	XX
75	00 05	00 12	0012	0	0003	0034	10	00 05	0	0	0	1	1	0	XX	XX
76	00 06	00 11	0011	0	0003	0034	10	00 06	0	0	0	1	1	0	XX	XX
77	00 07	00 10	0010	0	0003	0034	10	00 07	0	0	0	1	1	0	XX	XX
78	00 10	00 07	0007	0	0003	0034	10	00 10	0	0	1	1	1	0	XX	XX
79	00 11	00 06	0006	0	0003	0034	10	00 11	0	0	1	1	1	0	XX	XX
80	00 12	00 05	0005	0	0003	0034	10	00 12	0	0	1	1	1	0	XX	XX
81	00 13	00 04	0004	0	0003	0034	10	00 13	0	0	1	1	1	0	XX	XX
82	00 14	00 03	0003	0	0003	0034	10	00 14	0	0	1	1	1	0	XX	XX
83	00 15	00 02	0002	0	0003	0034	10	00 15	0	0	1	1	1	0	XX	XX
84	00 16	00 01	0001	0	0003	0034	10	00 16	0	0	1	1	1	0	XX	XX
85	00 17	00 00	0000	0	0003	0034	10	00 17	0	1	1	0	0	0	XX	XX
86	00 00	00 17	0017	0	0003	0034	10	00 00	0	0	0	1	1	1	XX	XX
87	00 01	00 16	0016	0	0003	0034	10	00 01	0	0	0	1	1	0	XX	XX
88	00 02	00 15	0015	0	0003	0034	10	00 02	0	0	0	1	1	0	XX	XX
89	00 03	00 14	0014	0	0003	0034	10	00 03	0	0	0	1	1	0	XX	XX
90	00 04	00 13	0013	0	0003	0034	10	00 04	0	0	0	1	1	0	XX	XX
91	00 05	00 12	0012	0	0003	0034	10	00 05	0	0	0	1	1	0	XX	XX
92	00 06	00 11	0011	0	0003	0034	10	00 06	0	0	0	1	1	0	XX	XX
93	00 07	00 10	0010	0	0003	0034	10	00 07	0	0	0	1	1	0	XX	XX
94	00 10	00 07	0007	0	0003	0034	10	00 10	0	0	1	1	1	0	XX	XX
95	00 11	00 06	0006	0	0003	0034	10	00 11	0	0	1	1	1	0	XX	XX
96	00 12	00 05	0005	0	0003	0034	10	00 12	0	0	1	1	1	0	XX	XX
97	00 13	00 04	0004	0	0003	0034	10	00 13	0	0	1	1	1	0	XX	XX
98	00 14	00 03	0003	0	0003	0034	10	00 14	0	0	1	1	1	0	XX	XX
99	00 15	00 02	0002	0	0003	0034	10	00 15	0	0	1	1	1	0	XX	XX
100	00 16	00 01	0001	0	0003	0034	10	00 16	0	0	1	1	1	0	XX	XX
101	00 17	00 00	0000	0	0003	0034	10	00 17	0	1	1	0	0	0	XX	XX
102	00 17-	00 00	0000	0	0001	0034	11	00 ZZ	0	1	1	0	0	0	XX	XX

SET 5

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	$\overline{OE}$	Y_{3-0}	P	G	F_3	$\overline{CN4}$	$\overline{OVR}$	F_0	Q_{30}	R_{30}
103	00 00	0017	00 17	0	0001	003 4	11	00 ZZ	0	0	0	1	1	1	XX	XX
104	00 00	0000	00 04	0	0002	003 7	10	00 00	0	0	0	1	1	0	XX	XX
105	00 00	0000	00 04	0	0002	003 7	00	00 00	0	0	0	1	1	0	XX	XX
106	00 00	0000	00 04	0	0002	003 7	10	00 04	0	0	0	1	1	0	XX	XX
107	00 00	0000	00 00	0	0001	003 2	10	00 17	0	1	1	0	0	0	XX	XX
108	00 00	0000	00 00	0	0001	003 2	00	00 17	0	1	1	0	0	0	XX	XX
109	00 00	0000	00 00	0	0001	003 2	10	00 17	0	1	1	0	0	0	ZZ	ZZ
110	00 00	0000	00 02	0	0000	003 7	10	00 02	0	0	0	1	1	0	XX	XX
111	00 00	0000	00 02	0	0000	003 7	00	00 02	0	0	0	1	1	0	XX	XX
112	00 00	0000	00 02	0	0000	003 7	10	00 02	0	0	0	1	1	0	XX	XX
113	00 00	0017	00 00	0	0001	000 0	10	00 06	1	1	0	0	0	0	XX	XX
114	00 00	0017	00 00	0	0001	0000	00	00 06	1	1	0	0	0	0	XX	XX
115	00 00	0017	00 00	0	0001	0000	10	00 06	1	1	0	0	0	0	ZZ	ZZ
116	00 17	0000	00 00	0	0001	0000	10	00 01	0	0	0	1	0	0	XX	XX
117	00 17	0000	00 00	0	0001	0000	00	00 01	0	0	0	1	0	0	XX	XX
118	00 17	0000	00 00	0	0001	0000	10	00 01	0	0	0	1	0	0	XX	XX
119	00 00	0017	00 01	0	0002	0006	10	00 04	1	1	0	0	0	0	XX	XX
120	00 00	0017	00 01	0	0002	0006	00	00 04	1	1	0	0	0	0	XX	XX
121	00 00	0017	00 01	0	0002	0006	10	00 04	1	1	0	0	0	0	ZZ	ZZ
122	00 17	0000	00 00	0	0003	0000	10	00 05	1	1	0	0	0	0	XX	XX
123	00 17	0000	00 00	0	0003	0000	00	00 05	1	1	0	0	0	0	XX	XX
124	00 17	0000	00 00	0	0003	0000	10	00 05	1	1	0	0	0	0	ZZ	ZZ
125	00 00	0017	00 00	0	0001	0000	10	00 07	1	1	0	0	0	0	XX	XX
126	00 00	0017	00 00	0	0001	0000	00	00 07	1	1	0	0	0	0	XX	XX
127	00 00	0017	00 00	0	0001	0000	10	00 07	1	1	0	0	0	0	XX	XX
128	00 00	0017	00 17	0	0006	0045	10	00 05	0	0	0	1	1	0	0Z	0Z
129	00 00	0017	00 17	0	0006	0045	10	00 05	0	0	0	1	1	0	01	00
130	00 00	0017	00 17	0	0006	0045	00	00 05	0	0	0	1	1	0	01	00
131	00 00	0017	00 17	0	0006	0045	10	00 05	0	0	0	1	1	0	01	00
132	00 17	0017	00 17	1	0004	0053	10	00 05	0	0	0	1	1	0	Z1	Z0
133	00 17	0017	00 17	1	0004	0053	10	00 05	0	0	0	1	1	0	11	00
134	00 17	0017	00 17	1	0004	0053	00	00 05	0	0	0	1	1	0	11	00
135	00 17	0017	00 17	1	0004	0053	10	00 02	0	0	0	1	1	0	10	01
136	00 17	0017	00 17	1	0005	0053	10	00 05	0	0	0	1	1	0	Z0	Z1

SET 5

Test No.	A_{3-0}	B_{3-0}	D_{3-0}	C_N	I876	I_{5-0}	CP OE	Y_{3-0}	P	G	F_3	CN_4	OVR	F_0	Q_{30}	R_{30}
137	0017	0017	0017	1	0005	0053	10	0005	0	0	0	1	1	0	00	01
138	0017	0017	0017	1	0005	0053	00	0005	0	0	0	1	1	0	00	01
139	0017	0017	0017	1	0005	0050	10	0002	0	0	0	1	1	0	00	00
140	0017	0017	0017	1	0004	0053	10	0002	0	0	0	1	1	0	00	10
141	0017	0017	0017	1	0004	0053	00	0002	0	0	0	1	1	0	00	10
142	0017	0017	0017	1	0004	0053	10	0011	0	0	1	1	1	0	01	11
143	0017	0017	0017	1	0005	0053	10	0011	0	0	1	1	1	0	11	10
144	0017	0017	0017	1	0005	0053	00	0011	0	0	1	1	1	0	11	10
145	0017	0017	0017	1	0005	0053	10	0004	0	0	0	1	1	0	11	11
146	0017	0017	0017	1	0001	0032	10	0005	0	0	0	1	1	0	XX	XX
147	0017	0017	0017	1	0001	0032	00	0005	0	0	0	1	1	0	XX	XX
148	0017	0017	0017	1	0001	0032	10	0005	0	0	0	1	1	0	XX	XX
149	0017	0017	0017	1	0006	0053	10	0004	0	0	0	1	1	0	00	01
150	0017	0017	0017	1	0006	0053	00	0004	0	0	0	1	1	0	00	01
151	0017	0017	0017	1	0006	0053	10	0011	0	0	1	1	1	0	10	11
152	0017	0017	0017	1	0007	0053	10	0011	0	0	1	1	1	0	12	12
153	0017	0017	0017	1	0007	0053	10	0011	0	0	1	1	1	0	11	10
154	0017	0017	0017	1	0007	0053	00	0011	0	0	1	1	1	0	11	10
155	0017	0017	0017	1	0007	0053	10	0002	0	0	0	1	1	0	11	00
156	0017	0017	0017	1	0006	0053	10	0002	0	0	0	1	1	0	11	01
157	0017	0017	0017	1	0006	0053	00	0002	0	0	0	1	1	0	11	01
158	0017	0017	0017	1	0006	0053	10	0005	0	0	0	1	1	0	01	01
159	0017	0017	0017	1	0007	0053	10	0005	0	0	0	1	1	0	00	00
160	0017	0017	0017	1	0007	0053	00	0005	0	0	0	1	1	0	00	00
161	0017	0017	0017	1	0007	0053	10	0012	0	0	1	1	1	0	00	10
162	0017	0017	0017	1	0006	0032	10	0005	0	0	0	1	1	0	00	00
163	0017	0017	0017	1	0006	0032	00	0005	0	0	0	1	1	0	00	00
164	0017	0017	0017	1	0006	0032	10	0012	0	0	1	1	1	0	10	10
165	0017	0017	0017	1	0004	0076	10	0012	1	1	1	0	0	0	00	00
166	0017	0017	0017	1	0004	0076	00	0012	1	1	1	0	0	0	00	00
167	0017	0017	0017	1	0004	0076	10	0005	1	1	0	0	0	0	01	01
168	0000	0017	0017	1	0006	0076	10	0005	1	1	0	0	0	0	00	00
169	0000	0017	0017	1	0006	0076	00	0005	1	1	0	0	0	0	00	00
170	0000	0017	0017	1	0006	0076	10	0012	1	1	1	0	0	0	10	10

v. Switching Speed Test Changes

The information on the following pages was included in the slash sheet by GE to clarify the switching speed tests.

The algorithms for the input data patterns were rewritten so that they are no longer tester-oriented. Duplicate patterns were eliminated. Three new patterns were added for set-up time measurements that were omitted from the preliminary slash sheet. Patterns 1, 3, and 4 were modified so that previously unchecked paths would be exercised.

Flowcharts were written for the patterns and the description of the terminology used in the algorithms was revised.

The format for the slash sheet Table III B was changed to that used in other slash sheets and much information was added to it.

Switching Time Test Patterns (Algorithms) For Group (A) Tests, Subgroups 9, 10, and 11

The following pages contain the flow charts and algorithms for the input data patterns used during the switching speed tests.

The term CALL TEST (V_1, V_2, V_3, V_4, V_5, V_6, V_7) is used to define the states applied to each input of the device during one test cycle. The parameters V_1 through V_7 are in decimal notation and represent the binary states applied to the inputs as follows:

Variable	Signals
V_1	$A_3 - A_0$
V_2	$B_3 - B_0$
V_3	$D_3 - D_0$
V_4	C_n
V_5	$I_8 - I_6$
V_6	$I_5 - I_3$
V_7	$I_2 - I_0$

For example:
CALL TEST (0,1,2,0,3,4,5) would initiate a test cycle in which

$A_3 - A_0$	=	0000
$B_3 - B_0$	=	0001
$D_3 - D_0$	=	0010
C_n	=	0
$I_8 - I_6$	=	011
$I_5 - I_3$	=	100
$I_2 - I_0$	=	101

Numerous test cycles are implemented by using a LOOP I = n_1, n_2 statement in conjunction with the CALL TEST statement. This causes $n_2 - n_1 + 1$ test cycles to be performed. The parameter I can be assigned to one or more of the variables V_1 through V_7 thus allowing that variable to be cycled from n_1 to n_2. The variables V_1 through V_7 can also be defined by a logical expression -e.g. I AND 1.

A test cycle is performed each time a CALL TEST statement appears. The timing of the test cycle varies depending on the parameter being measured. Figures 7 through 12 show the timing relationships for the various tests performed.

```
CALL TEST (0,0,0,0,0,3,7)

LOOP I = 0,15
CALL TEST (0,I,I,0,3,3,7)
END I

LOOP I = 0,15
LOOP J = 0,15
CALL TEST (I,0,J,0,3,0,5)
CALL TEST (I,0,J,0,1,3,3)
CALL TEST (I,0,J,0,4,0,5)
CALL TEST (I,0,J,0,6,0,5)
END J,  END I

LOOP I = 0,15
CALL TEST (0,0,I,0,0,3,7)
CALL TEST (0,0,0,0,1,3,2)
END I
```

There are 1073 tests in this group.

Figure 14A . Test Pattern 1

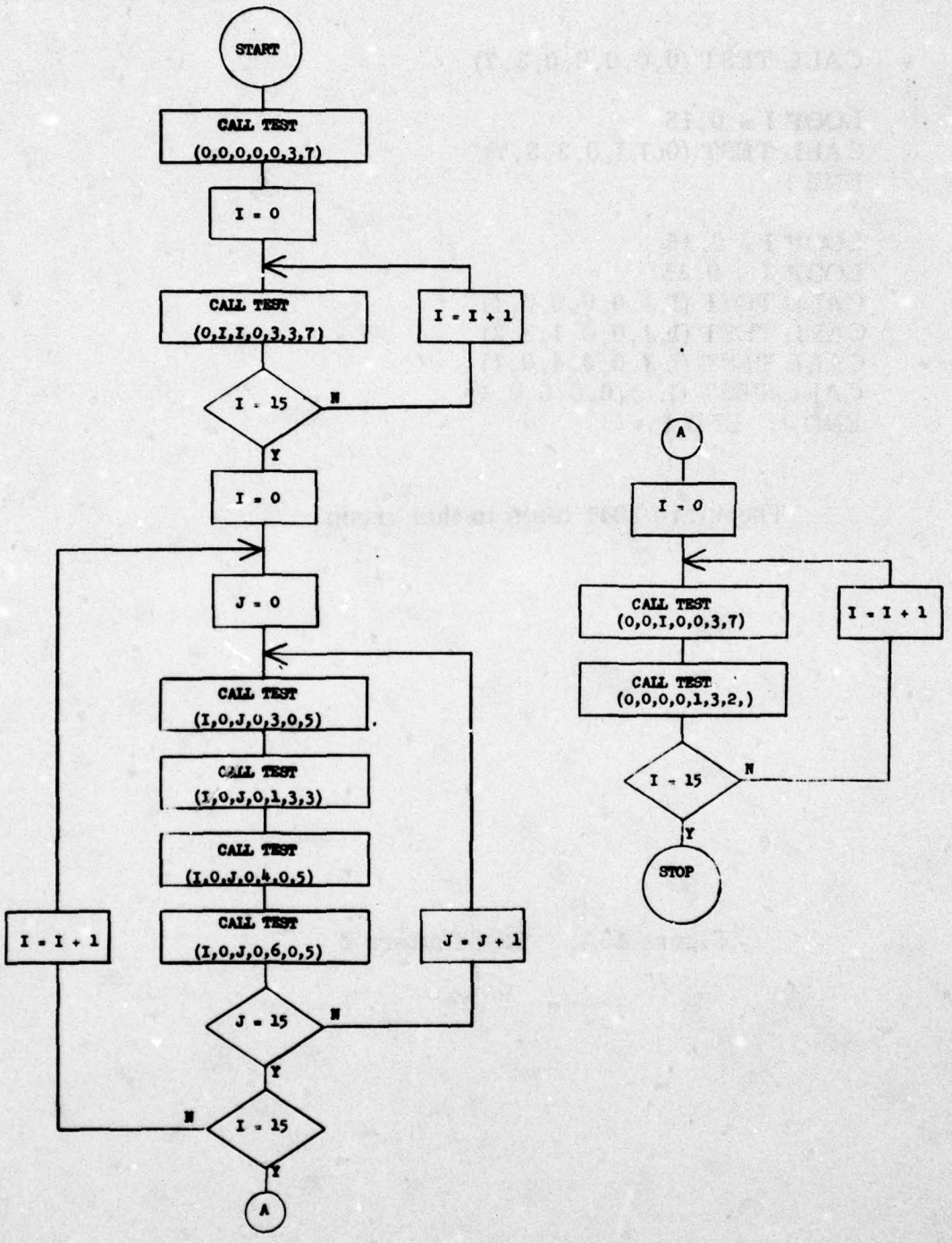


Figure 14B. Flowchart for test pattern 1

```
CALL TEST (0,0,0,0,0,0,3,7)

LOOP I = 0,15
CALL TEST (0,I,I,0,3,3,7)
END I

LOOP I = 0,15
LOOP J = 0,15
CALL TEST (I,J,0,0,0,0,1)
CALL TEST (I,J,0,0,1,3,2)
CALL TEST (I,J,0,0,4,0,1)
CALL TEST (I, J,0,0,6,0,1)
END J.  END I
```

There are 1041 tests in this group

Figure 15A. Test Pattern 2

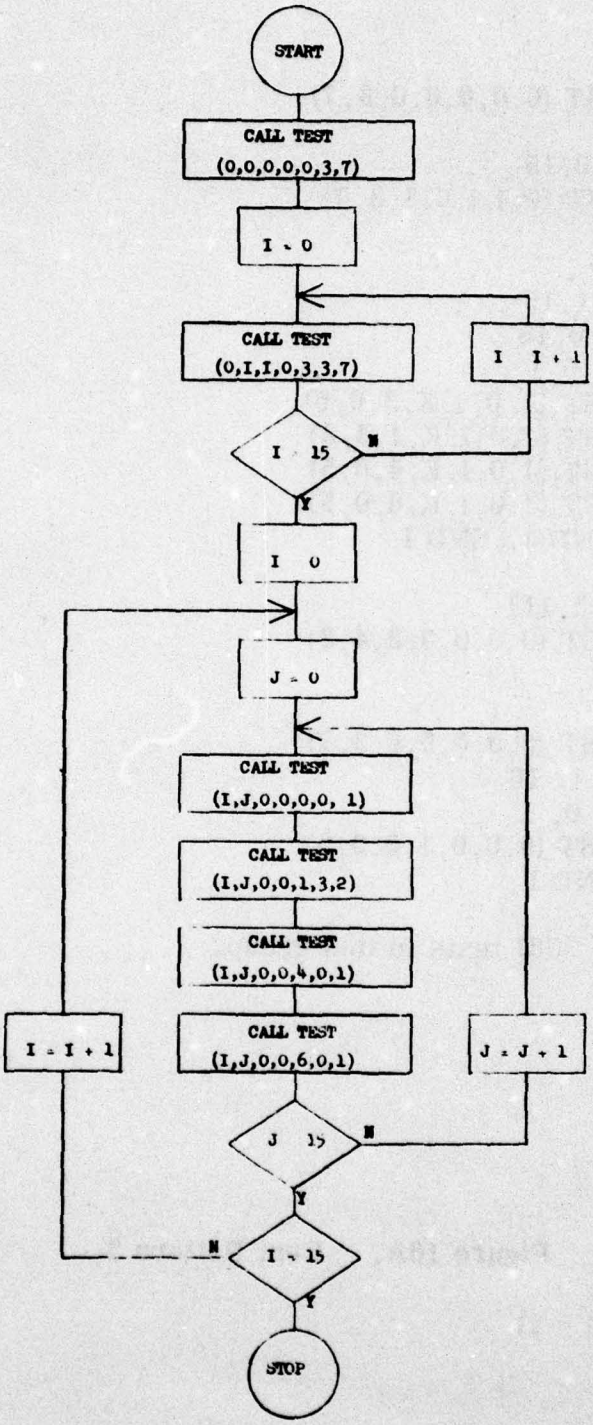


Figure 15B. Flowchart for test pattern 2

```
CALL TEST (0,0,0,0,0,3,7)

LOOP I = 0,15
CALL TEST (0,I,I,0,3,3,7)
END I

LOOP I = 1,15
LOOP J = 0,15
LOOP K = 0,1
CALL TEST (J,0,I,K,3,0,5)
CALL TEST (J,0,I,K,1,3,3)
CALL TEST (J,0,I,K,4,0,5)
CALL TEST (J,0,I,K,6,0,5)
END K, END J, END I

LOOP I = 1,111
CALL TEST (0,0,0,0,2,4,2)
END I

CALL TEST (0,0,0,0,0,3,7)
LOOP I = 1, 16
LOOP J = 0, 1
CALL TEST (0,0,0,J,0,0,6)
END J, END I
```

There are 2081 tests in this group.

Figure 16A. Test Pattern 3

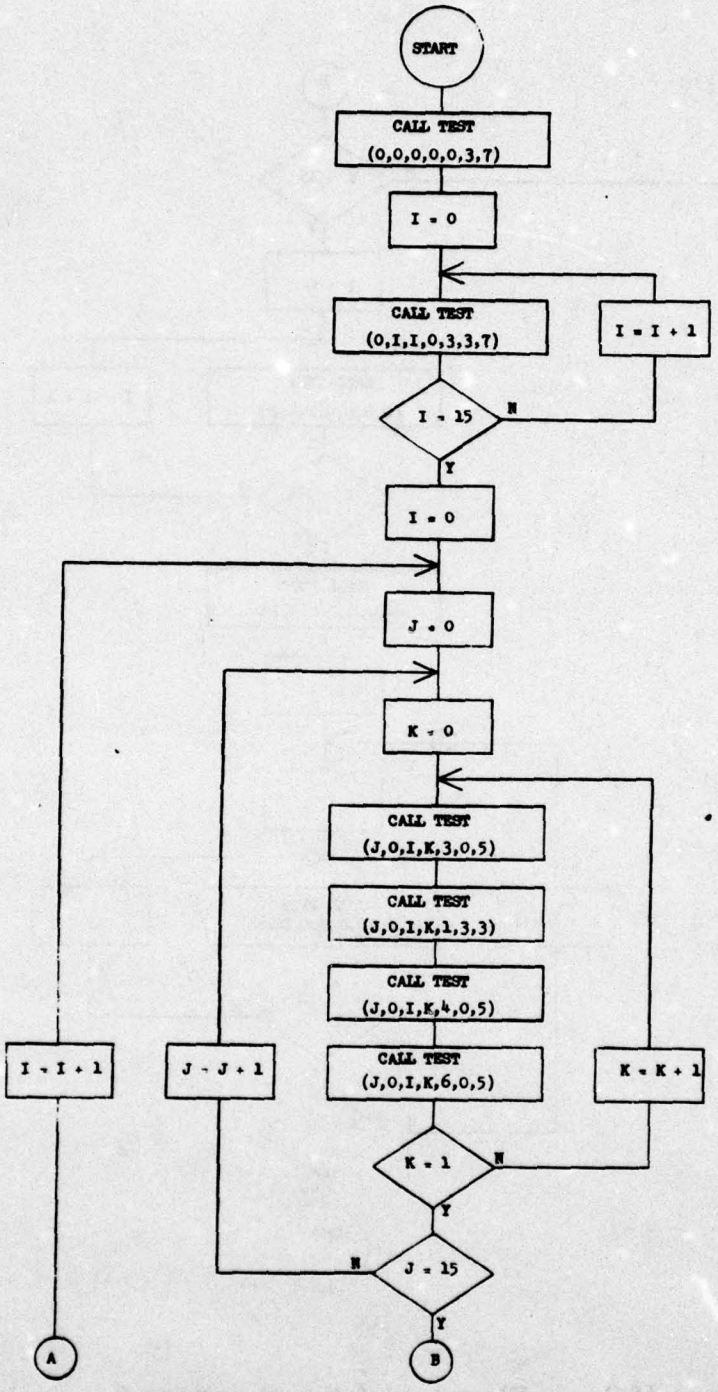


Figure 16B Flowchart for test pattern 3

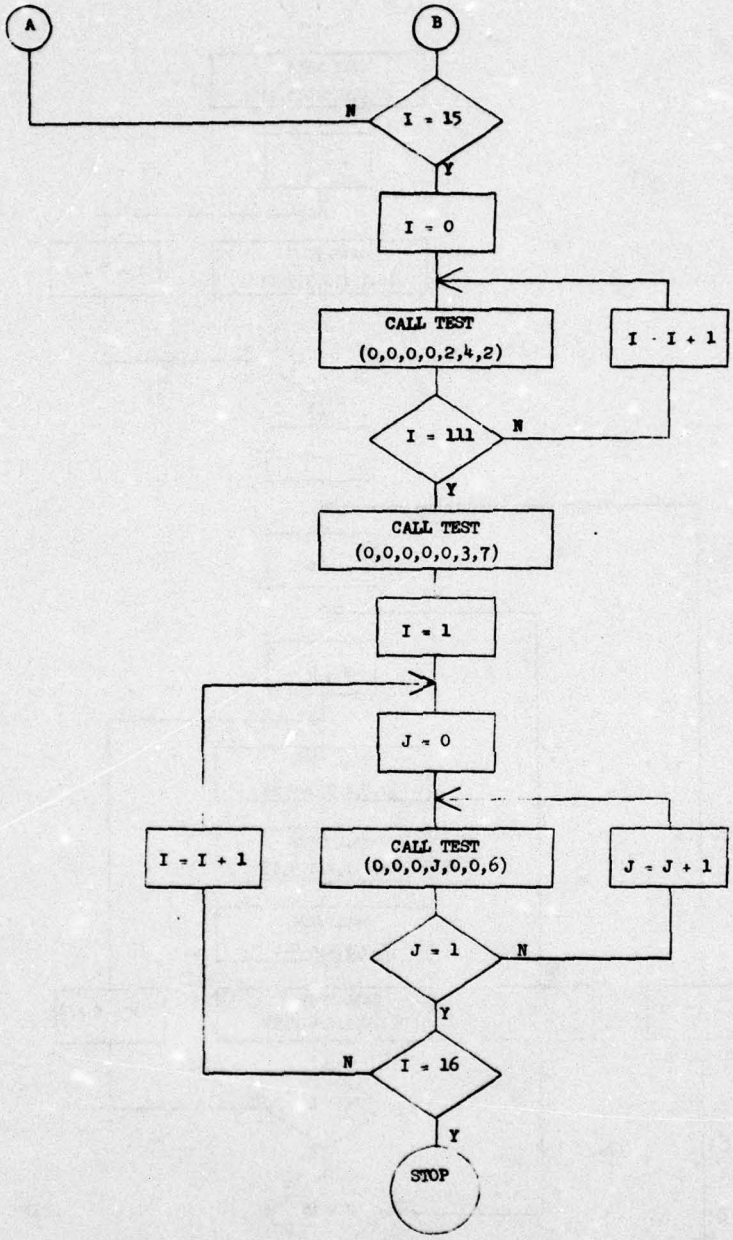


Figure 16C. Flowchart for test pattern 3, concluded

```
CALL TEST (10,0,15,0,0,3,7)
CALL TEST (0,10,10,0,3,3,7)
CALL TEST (10,0,0,0,3,3,7)

LOOP I = 0,7
CALL TEST (10,0,5,0,1,6,I)
END I

LOOP I = 0,7
CALL TEST (10,0,5,0,1,7,I)
END I

LOOP I = 0,7
CALL TEST (10,0,15,0,0,3,7)
CALL TEST (0,10,10,0,3,3,7)
CALL TEST (10,0,0,0,3,3,7)
CALL TEST (10,0,5,0,4,1,I)
END I

LOOP I = 0,7
CALL TEST (10,0,15,0,0,3,7)
CALL TEST (0,10,10,0,3,3,7)
CALL TEST (10,0,0,0,3,3,7)
CALL TEST (10,0,5,0,4,1,I)
END I

DIMENSION ARRAY XXX (8)
INITIALIZE XXX (8) /7,5,4,0,1,3,2,6 /

LOOP I = 0,15
CALL TEST (I,I,I,0,3,3,7)
END I

LOOP I = 0,15
LOOP J = 1,8
CALL TEST (I,I,0,0,1,XXX(J), 1)
END J, END I

LOOP I = 0,15
LOOP J = 1,8
CALL TEST (15-I,I,0,0,1,XXX (J),1)
END J, END I
```

Figure 17A. Test pattern 4

```
LOOP I = 0,15
CALL TEST (I,I,I,0,3,3,7)
LOOP J = 1,8
CALL TEST (I,I,0,0,4,XXX(J),1)
END J, END I
```

Figure 17A. Test pattern 4

```
LOOP I = 0,15
CALL TEST (I,I,I,0,3,3,7)
LOOP J = 1,8
CALL TEST (I,I,0,0,6,XXX(J),1)
END J, END I

CALL TEST (0,10,10,0,3,3,7)
CALL TEST (10,10,10,0,0,3,7)

LOOP I = 0,2
CALL TEST (10,10,5,0,Iand 1,3,7)
CALL TEST (10,10,15,0,6,3,7)
CALL TEST (10,10,15,0,4,3,7)
END I

CALL TEST (10,0,5,0,0,3,7)
CALL TEST (10,10,10,0,3,3,7)

LOOP I = 0,7
CALL TEST (0,0,0,0,3,3,7)
CALL TEST (10,0,5,0,1,6,I)
CALL TEST (10,0,5,0,2,6,I)
END I

LOOP I = 0,15
CALL TEST (I,I,I,0,3,3,7)
END I

LOOP I = 0,15
LOOP J = 0,7
CALL TEST (I,I,0,0,1,J,1)
CALL TEST (I,I,0,0,2,J,1)
CALL TEST (I,I,0,0,3,3,7)
END J, END I
CALL TEST (10,10,10,0,3,3,7)
CALL TEST (10,10,10,0,0,3,7)
CALL TEST (10,10,10,0,3,3,7)
CALL TEST (10,10,10,0,0,3,7)
CALL TEST (10,10,10,0,4,3,2)
CALL TEST (10,10,10,0,4,3,3)
CALL TEST (10,10,10,0,6,3,2)
CALL TEST (10,10,10,0,6,3,3)
CALL TEST (10,10,10,0,4,3,2)
CALL TEST (10,10,10,0,4,3,3)
CALL TEST (10,10,10,0,6,3,2)
CALL TEST (10,10,10,0,6,3,3)
```

Figure 17B. Test pattern 4, cont'd

```
LOOP I = 0,15
LOOP J = 1,16
CALL TEST (0,0,I,0,4,0,6)
END J, END I

LOOP I = 0,15
LOOP J = 1,16
CALL TEST (0,0,I,0,6,0,6)
END J, END I

CALL TEST (0,0,0,0,0,3,7)
LOOP I = 0,15
LOOP J = 1,16
CALL TEST (0,0,I,0,0,0,6)
END J, END I

LOOP I = 0,15
CALL TEST (0,I,I,0,3,3,7)
END I

LOOP I = 0,15
LOOP J = 0,15
CALL TEST (I,I,J,1,3,0,5)
END J, END I
```

There are 2131 tests in this group.

Figure 17C. Test pattern 4, concluded

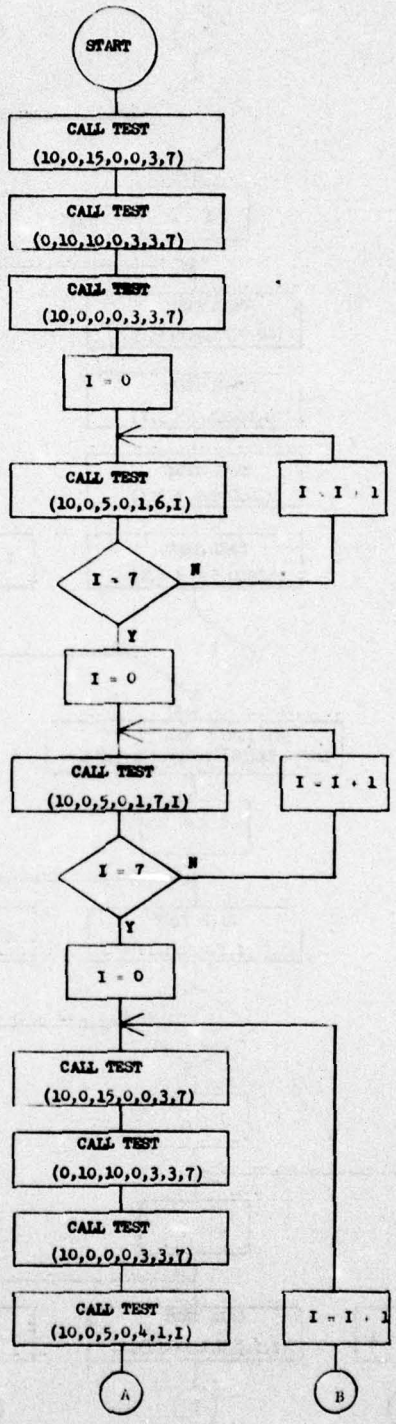


Figure 17D. Flowchart for test pattern 4

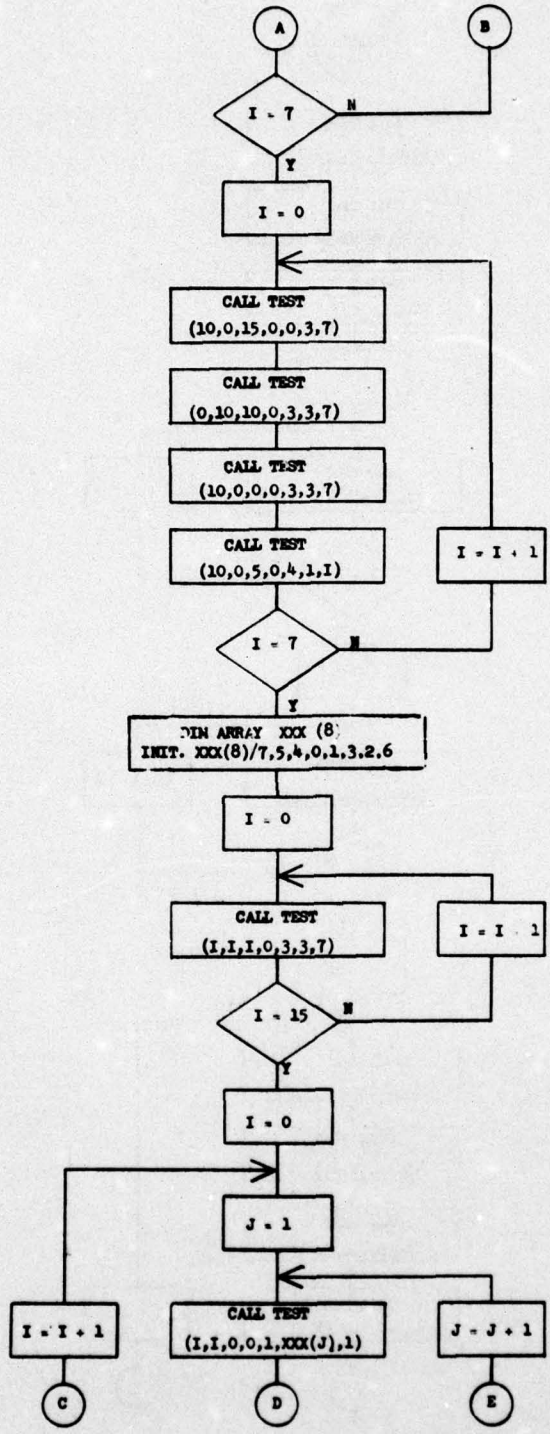


Figure 17E. Flowchart for test pattern 4, cont'd

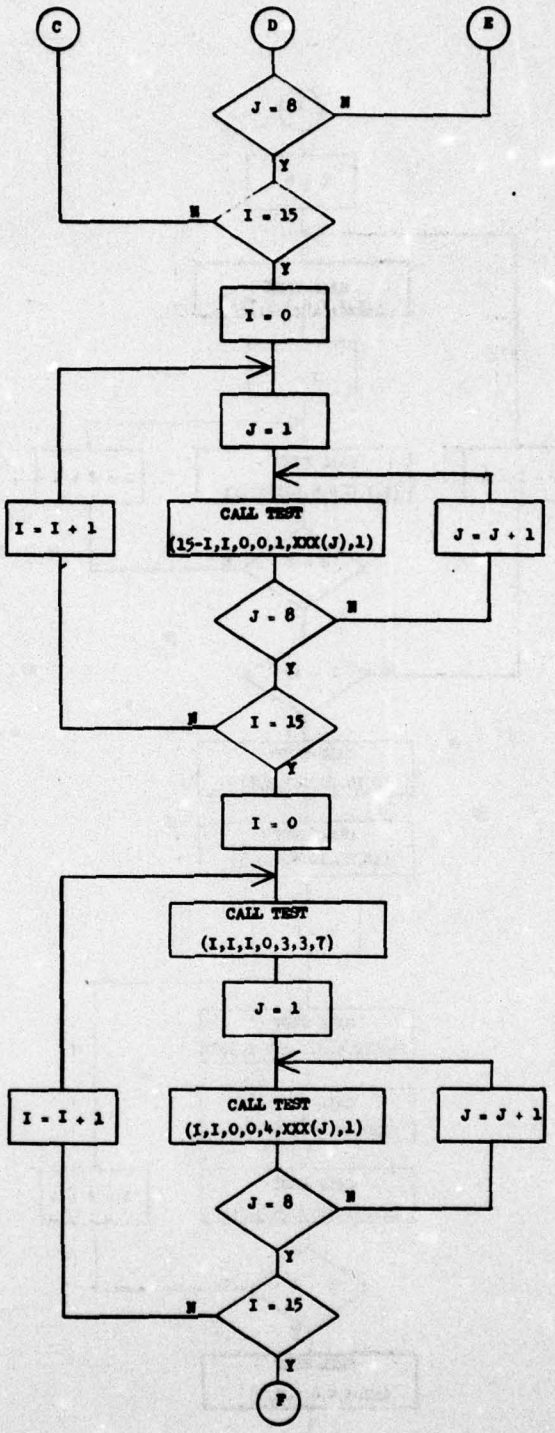


Figure 17F. Flowchart for test pattern 4, cont'd

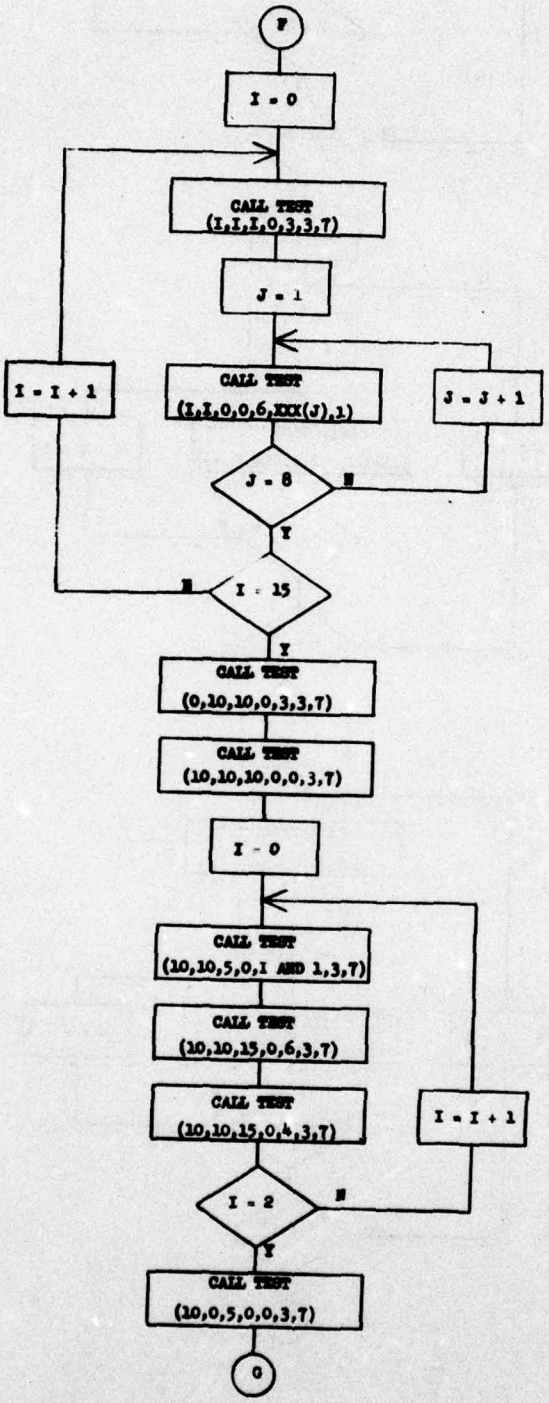


Figure 17G. Flowchart for test pattern 4 , cont'd

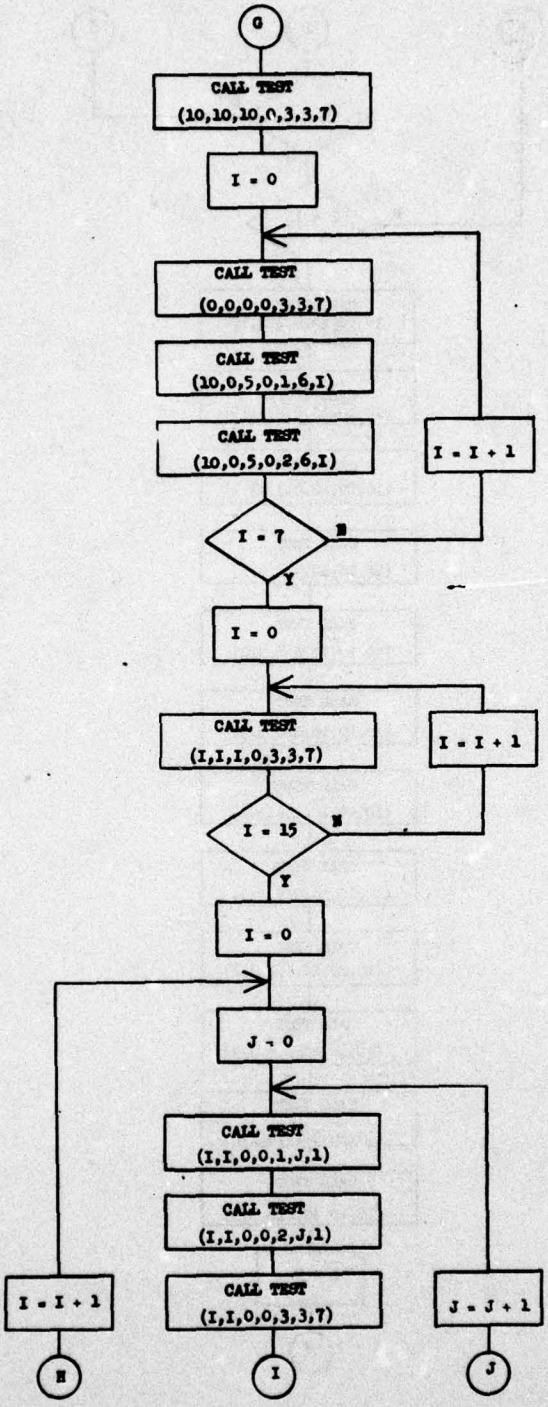


Figure 17H. Flowchart for test pattern 4, cont'd

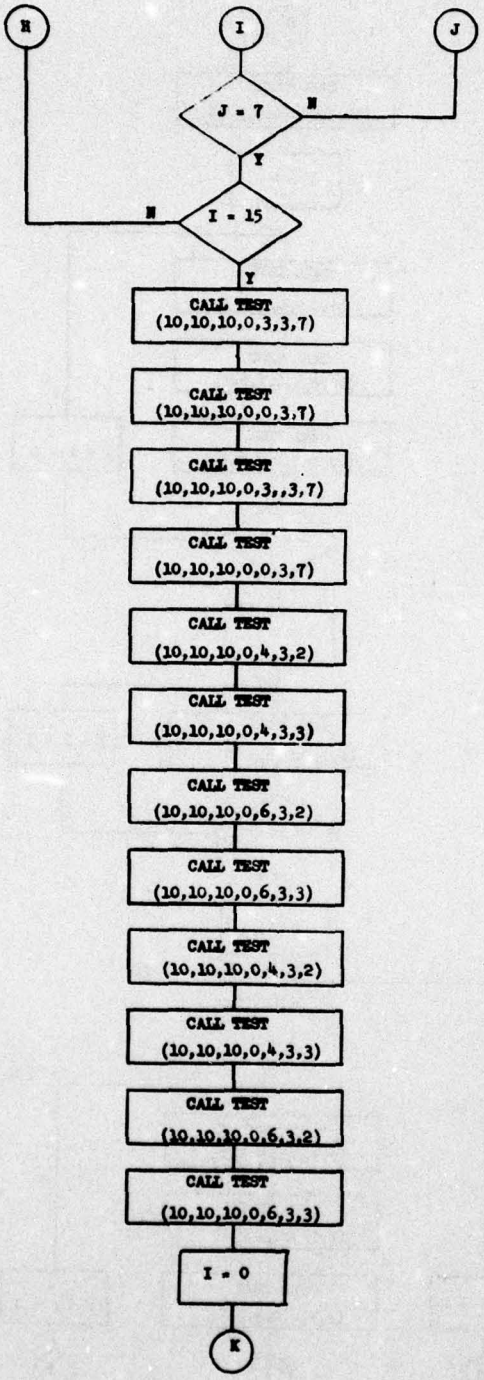


Figure 17I. Flowchart for test pattern 4, cont'd

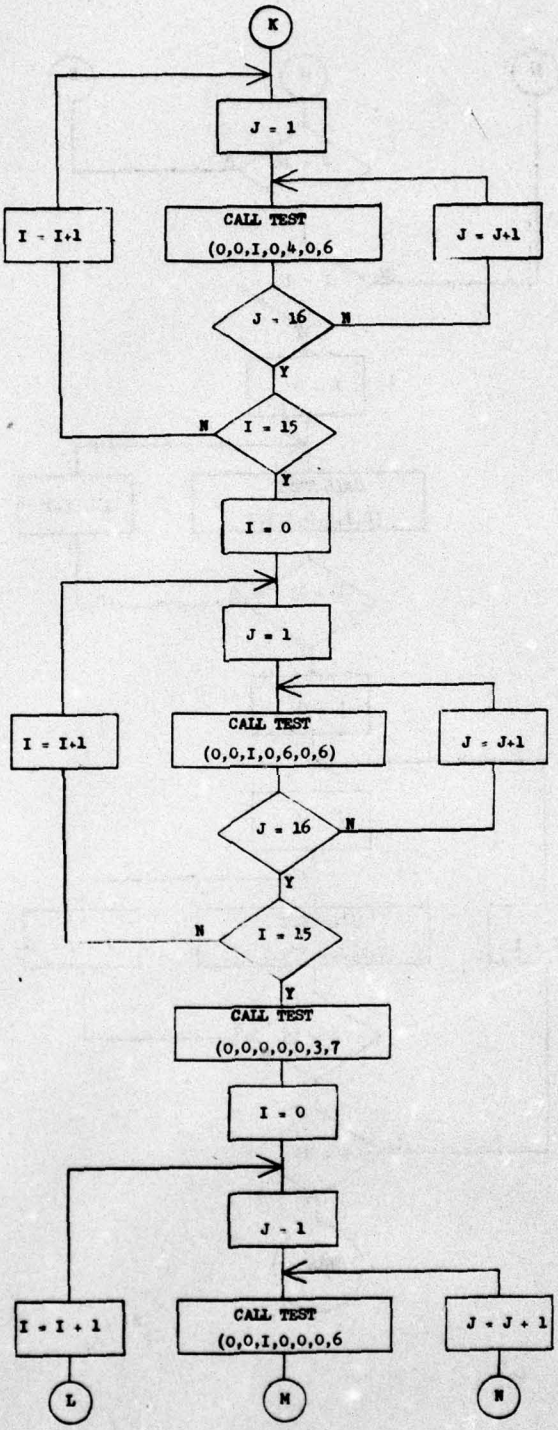


Figure 17J. Flowchart for test pattern 4, cont'd

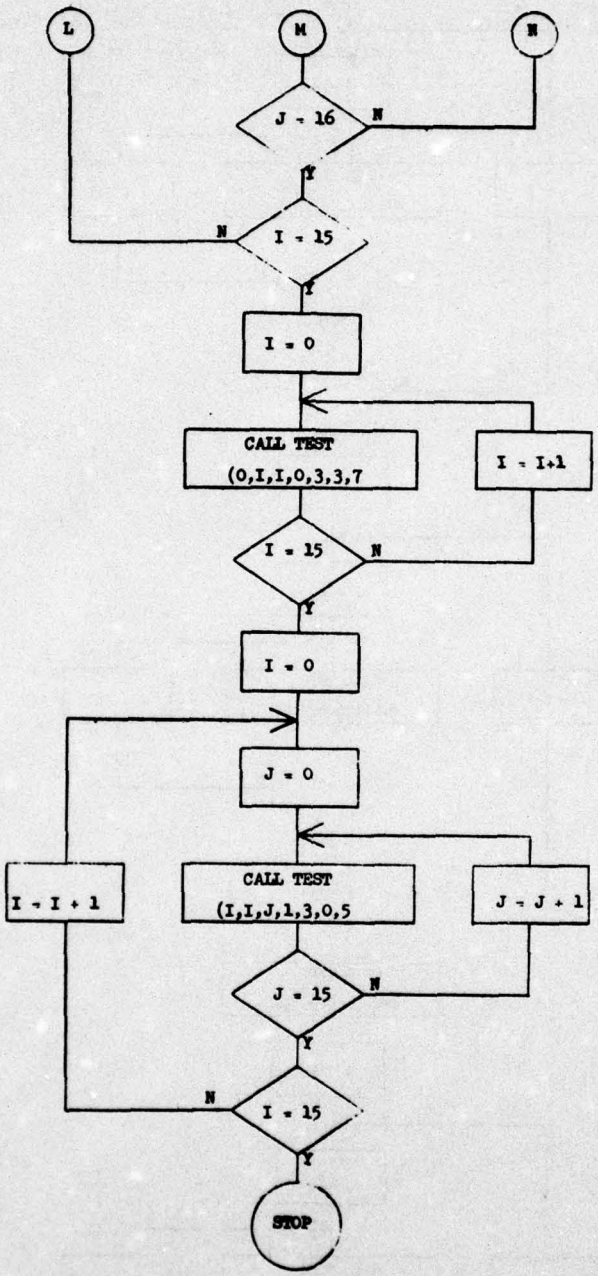


Figure 17K. Flowchart for test pattern 4, concluded

This pattern consists of the A Port Galpat Bypassing the ALU portion of the functional test. It is identified as Test Group 11, Test Numbers 2035 through 3054 of Table V.

Figure 18. Test pattern 5

```
LOOP I = 0,15
CALL TEST (I,I,I,0,2,3,7)
END I

LOOP I = 0,15
CALL TEST (I,I,15-I,0,2,3,7)
END I

LOOP I = 0,15
CALL TEST (I,I,I,0,2,3,7)
END I
```

There are 48 tests in this group.

Figure 19A. Test pattern 6

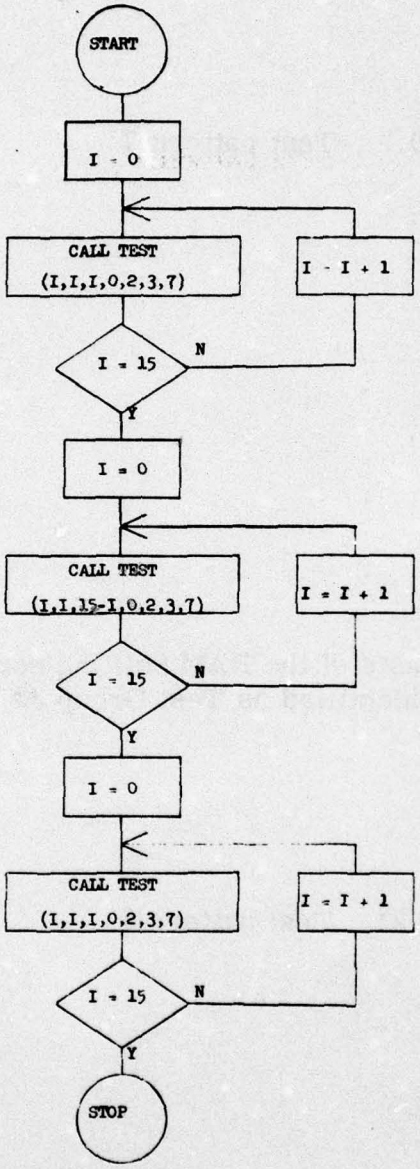


Figure 19B. Flowchart for test pattern 6

This pattern consists of the Q Register Shifting portion of the functional test. It is identified as Test Group 33, Test Numbers 2464 to 2610.

Figure 20. Test pattern 7

This pattern consists of the RAM Shifting portion of the functional test. It is identified as Test Group 33, Test Numbers 2611 to 2735.

Figure 21. Test pattern 8

vi. Changes to Table III

Table III was rewritten to make it compatible with the measurement techniques established on Mil-M-38510/400 and /420. Also the algorithmic approach to the dynamic testing and the different pinouts on the DIP vs. Flatpack packages required additional format changes. When the table was rewritten, the terminology was also changed to reflect Mil-M-38510.

TABLE III B GROUP (A) TESTS - SUBGROUPS 9,10,11,7,8

SYMBOL	TEST NUMBER	TEST PATTERN NUMBER	WAVEFORM FIGURE	MEASUREMENT TERMINALS (Q) DIP		MEASUREMENT TERMINALS (R) FLATPACK		TEST LIMITS SUBGROUP 9 +25°C		TEST LIMITS SUBGROUP 10 +125°C		TEST LIMITS SUBGROUP 11 -55°C		UNITS
				INPUT UNDER TEST	OUTPUT UNDER TEST	INPUT UNDER TEST	OUTPUT UNDER TEST	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL1} t_{PLH1}	171	1,2	7	1 - 4	36-39	38-41	33-36				90		90	ns
t_{PHL2} t_{PLH2}	172	1,2	7	1 - 4	31	38-41	28				80		80	ns
t_{PHL3} t_{PLH3}	173	1,2	7	1 - 4	33	38-41	30				80		80	ns
t_{PHL4} t_{PLH4}	174	1,2	7	1 - 4	32,35	38-41	29,32				80		80	ns
t_{PHL5} t_{PLH5}	175	1,2	7	1 - 4	11	38-41	7				90		90	ns
t_{PHL6} t_{PLH6}	176	1,2	7	1 - 4	34	38-41	31				90		90	ns
t_{PHL7} t_{PLH7}	177	1,2	7	1 - 4	8,9	38-41	3,5				100		100	ns
t_{PHL8} t_{PLH8}	178	2	7	17-20	36-39	14-17	33-36				90		90	ns
t_{PHL9} t_{PLH9}	179	2	7	17-20	31	14-17	28				80		80	ns
t_{PHL10} t_{PLH10}	180	2	7	17-20	33	14-17	30				80		80	ns

TABLE III B GROUP (A) TESTS SUBGROUPS 9,10,11,7,8 (Con't.)

SYMBOL	TEST NUMBER	TEST PATTERN NUMBER	WAVEFORM FIGURE	MEASUREMENT TERMINALS (Q) DIP		MEASUREMENT TERMINALS (R) FLATPACK		TEST LIMITS SUBGROUP 9 +25°C		TEST LIMITS SUBGROUP 10 +125°C		TEST LIMITS SUBGROUP 11 -55°C		UNITS
				INPUT UNDER TEST	OUTPUT UNDER TEST	INPUT UNDER TEST	OUTPUT UNDER TEST	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL11} t_{PLH11}	181	2	7	17-20	32,35	14-17	29,32				80		80	ns
t_{PHL12} t_{PLH12}	182	2	7	17-20	11	14-17	7				90		90	ns
t_{PHL13} t_{PLH13}	183	2	7	17-20	34	14-17	31				90		90	ns
t_{PHL14} t_{PLH14}	184	2	7	17-20	8,9	14-17	3,5				100		100	ns
t_{PHL15} t_{PLH15}	185	1	7	22-25	36-39	19-22	33-36				60		60	ns
t_{PHL16} t_{PLH16}	186	1	7	22-25	31	19-22	28				50		50	ns
t_{PHL17} t_{PLH17}	187	1	7	22-25	33	19-22	30				50		50	ns
t_{PHL18} t_{PLH18}	188	1	7	22-25	32,35	19-22	29,32				50		50	ns
t_{PHL19} t_{PLH19}	189	1	7	22-25	11	19-22	7				60		60	ns

TABLE III B GROUP (A) TESTS - SUBGROUPS 9,10,11,7,8 (Con't.)

SYMBOL	TEST NUMBER	TEST PATTERN NUMBER	WAVEFORM FIGURE	MEASUREMENT TERMINALS (Q) DIP		MEASUREMENT TERMINALS (R) FLATPACK		TEST LIMITS SUBGROUP 9 +25°C		TEST LIMITS SUBGROUP 10 +125°C		TEST LIMITS SUBGROUP 11 -55°C		UNITS
				INPUT UNDER TEST	OUTPUT UNDER TEST	INPUT UNDER TEST	OUTPUT UNDER TEST	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL20} t_{PLH20}	190	1	7	22-25	34	19-22	31				60		60	ns
t_{PHL21} t_{PLH21}	191	1	7	22-25	8,9	19-22	3,5				70		70	ns
t_{PHL22} t_{PLH22}	192	6	7	22-25	36-39	19-22	33-36				60		60	ns
t_{PHL23} t_{PLH23}	193	6	7	22-25	31	19-22	28				50		50	ns
t_{PHL24} t_{PLH24}	194	6	7	22-25	11	19-22	7				60		60	ns
t_{PHL25} t_{PLH25}	195	6	7	22-25	8,9	19-22	3,5				65		65	ns
t_{PHL26} t_{PLH26}	196	3	7	29	36-39	26	33-36				45		45	ns
t_{PHL27} t_{PLH27}	197	3	7	29	31	26	28				30		30	ns
t_{PHL28} t_{PLH28}	198	3	7	29	33	26	30				30		30	ns
t_{PHL29} t_{PLH29}	199	3	7	29	11	26	7				50		50	ns

TABLE III B GROUP (A) TESTS - SUBGROUPS 9,10,11,7,8 (Con't.)

SYMBOL	TEST NUMBER	TEST PATTERN NUMBER	WAVEFORM FIGURE	MEASUREMENT TERMINALS (Q) DIP		MEASUREMENT TERMINALS (R) FLATPACK		TEST LIMITS SUBGROUP 9 +25°C		TEST LIMITS SUBGROUP 10 +125°C		TEST LIMITS SUBGROUP 11 -55°C		UNITS
				INPUT UNDER TEST	OUTPUT UNDER TEST	INPUT UNDER TEST	OUTPUT UNDER TEST	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL30} t_{PLH30}	200	3	7	29	34	26	31				40		40	ns
t_{PHL31} t_{PLH31}	201	3	7	29	8,9	26	3,5				55		55	ns
t_{PHL32} t_{PLH32}	202	4	7	12-14	36-39	8-10	33-36				70		70	ns
t_{PHL33} t_{PLH33}	203	4	7	12-14	31	8-10	28				60		60	ns
t_{PHL34} t_{PLH34}	204	4	7	12-14	33	8-10	30				60		60	ns
t_{PHL35} t_{PLH35}	205	4	7	12-14	32,35	8-10	29,32				50		50	ns
t_{PHL36} t_{PLH36}	206	4	7	12-14	11	8-10	7				70		70	ns
t_{PHL37} t_{PLH37}	207	4	7	12-14	34	8-10	31				70		70	ns
t_{PHL38} t_{PLH38}	208	4	7	12-14	8,9	8-10	3,5				80		80	ns
t_{PHL39} t_{PLH39}	209	4	7	26-28	36-39	23-25	33-36				60		60	ns

TABLE III B GROUP (A) TESTS - SUBGROUPS 9,10,11,7,8 (Con't.)

SYMBOL	TEST NUMBER	TEST PATTERN NUMBER	WAVEFORM FIGURE	MEASUREMENT TERMINALS				TEST LIMITS						UNITS
				DIP		FLATPACK		SUBGROUP 9 +25°C		SUBGROUP 10 +125°C		SUBGROUP 11 -55°C		
				INPUT UNDER TEST	OUTPUT UNDER TEST	INPUT UNDER TEST	OUTPUT UNDER TEST	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL50} t_{PLH50}	220	4	8	15	33	11	30				80		80	ns
t_{PHL51} t_{PLH51}	221	4	8	15	32,35	11	29,32				70		70	ns
t_{PHL52} t_{PLH52}	222	4	8	15	11	11	7				90		90	ns
t_{PHL53} t_{PLH53}	223	4	8	15	34	11	31				80		80	ns
t_{PHL54} t_{PLH54}	224	4	8	15	8,9	11	3,5				90		90	ns
t_{PHL55} t_{PLH55}	225	4	8	15	16,21	11	13,18				50		50	ns
t_{PHZ1} t_{PLZ1}	226	3	12	40	36-39	37	33-36				30		30	ns
t_{PHZ2} t_{PLZ2}	227	4	12	5-7	8,9	1,2,42	3,5							ns
t_{PHZ3} t_{PLZ3}	228	4	12	5-7	16,21	1,2,42	13,18							ns

TABLE III B GROUP (A) TESTS - SUBGROUPS 9,10,11,7,8 (Con't.)

SYMBOL	TEST NUMBER	TEST PATTERN NUMBER	WAVEFORM FIGURE	MEASUREMENT TERMINALS				TEST LIMITS						UNITS
				DIP		FLATPACK		SUBGROUP 9 +25°C		SUBGROUP 10 +125°C		SUBGROUP 11 -55°C		
				INPUT UNDER TEST	OUTPUT UNDER TEST	INPUT UNDER TEST	OUTPUT UNDER TEST	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL40} t_{PLH40}	210	4	7	26-28	31	23-25	28				50		50	ns
t_{PHL41} t_{PLH41}	211	4	7	26-28	33	23-25	30				60		60	ns
t_{PHL42} t_{PLH42}	212	4	7	26-28	32,35	23-25	29,32				55		55	ns
t_{PHL43} t_{PLH43}	213	4	7	26-28	11	23-25	7				60		60	ns
t_{PHL44} t_{PLH44}	214	4	7	26-28	34	23-25	31				70		70	ns
t_{PHL45} t_{PLH45}	215	4	7	26-28	8,9	23-25	3,5				80		80	ns
t_{PHL46} t_{PLH46}	216	4	7	5-7	36-39	1,2,42	33-36				45		45	ns
t_{PHL47} t_{PLH47}	217	5	7	1-4	36-39	38-41	33-36				50		50	ns
t_{PHL48} t_{PLH48}	218	4	8	15	36-39	11	33-36				90		90	ns
t_{PHL49} t_{PLH49}	219	4	8	15	31	11	28				80		80	ns

TABLE III B GROUP (A) TESTS - SUBGROUPS 9,10,11,7,8 (Con't.)

SYMBOL	TEST NUMBER	TEST PATTERN NUMBER	WAVEFORM FIGURE	MEASUREMENT TERMINALS				TEST LIMITS						UNITS
				DIP		FLATPACK		SUBGROUP 9 +25°C		SUBGROUP 10 +125°C		SUBGROUP 11 -55°C		
				INPUT UNDER TEST	OUTPUT UNDER TEST	INPUT UNDER TEST	OUTPUT UNDER TEST	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PZL1} t_{PZH1}	229	3	12	40	36-39	37	33-36				40		40	ns
t_{PZL2} t_{PZH2}	230	4	12	5-7	8,9	1,2,42	3,5				50		50	ns
t_{PZL3} t_{PZH3}	231	4	12	5-7	16,21	1,2,42	13,18				50		50	ns
t_{SHL1} t_{SLH1}	232	1,2	9	1-4	8,9,11, 31-39	38-41	3,5,7, 28-36			110		110		ns
t_{SHL2} t_{SLH2}	233	1,2	9	1-4	8,9,11, 31-39	38-41	3,5,7, 28-36			30		30		ns
t_{SHL3} t_{SLH3}	234	2	9	17-20	8,9,11, 31-39	14-17	3,5,7, 28-36			110		110		ns
t_{SHL4} t_{SLH4}	235	2	9	17-20	8,9,11, 31-39	14-17	3,5,7, 28-36			30		30		ns
t_{SHL5} t_{SLH5}	236	6	11	17-20	8,9,11, 31-39	14-17	3,5,7, 28-36			15		15		ns
t_{SHL6} t_{SLH6}	237	1	10	22-25	8,9,11, 31-39	19-22	3,5,7, 28-36			75		75		ns

TABLE III B GROUP (A) TESTS - SUBGROUPS 9,10,11,7,8 (Con't.)

SYMBOL	TEST NUMBER	TEST PATTERN NUMBER	WAVEFORM FIGURE	MEASUREMENT TERMINALS				TEST LIMITS						UNITS
				DIP		FLATPACK		SUBGROUP 9 +25°C		SUBGROUP 10 +125°C		SUBGROUP 11 -55°C		
				INPUT UNDER TEST	OUTPUT UNDER TEST	INPUT UNDER TEST	OUTPUT UNDER TEST	MIN	MAX	MIN	MAX	MIN	MAX	
t_{SHL7} t_{SLH7}	238	6	11	22-25	8,9,11, 31-39	19-22	3,5,7, 28-36			65		65		ns
t_{SHL8} t_{SLH8}	239	3	10	29	8,9,11, 31-39	26	3,5,7, 28-36			60		60		ns
t_{SHL9} t_{SLH9}	240	4	10	12-14	8,9,11, 31-39	8-10	3,5,7, 28-36			85		85		ns
t_{SHL10} t_{SLH10}	241	4	10	26-28	8,9,11, 31-39	23-25	3,5,7, 28-36			85		85		ns
t_{SHL11} t_{SLH11}	242	4	10	5-7	8,9,11, 31-39	1,2,42	3,5,7, 28-36			30		30		ns
t_{SHL12} t_{SLH12}	243	4	10	16,21	11, 16,21, 31-39	13, 18	7, 13,18, 28-36			25		25		ns
t_{SHL13} t_{SLH13}	244	8	10	8,9	8,9,21, 31-39	3,5	3,5,7 28-36			25		25		ns
t_{HHL1} t_{HLH1}	245	1,2	7	1-4	8,9,11 31-39	38-41	3,5,7 28-36			0		0		ns
t_{HHL2} t_{HLH2}	246	2,6	7	17-20	8,9,11 31-39	14-17	3,5,7, 28-36			0		0		ns

TABLE III B GROUP (A) TESTS - SUBGROUPS 9,10,11,7,8 (Con't.)

SYMBOL	TEST NUMBER	TEST PATTERN NUMBER	WAVEFORM FIGURE	MEASUREMENT TERMINALS				TEST LIMITS						UNITS
				DIP		FLATPACK		SUBGROUP 9 +25°C		SUBGROUP 10 +125°C		SUBGROUP 11 -55°C		
				INPUT UNDER TEST	OUTPUT UNDER TEST	INPUT UNDER TEST	OUTPUT UNDER TEST	MIN	MAX	MIN	MAX	MIN	MAX	
t_{HHL3} t_{HLH3}	247	1,6	7	22-25	8,9,11, 31-39	19-22	3,5,7, 28-36			0		0		ns
t_{HHL4} t_{HLH4}	248	3	7	29	8,9,11, 31-39	26	3,5,7, 28-36			0		0		ns
t_{HHL5} t_{HLH5}	249	4	7	5-7, 12-14, 26-28	8,9,11, 31-39	1,2,8-10, 23-25, 42	3,5,7, 28-36			0		0		ns
t_{HHL6} t_{HLH6}	250	7	10	16,21	11,16,21 31-39	13,18	7,13, 18,28-36			0		0		ns
t_{HHL7} t_{HLH7}	251	8	10	8,9	8,9,21, 31-39	3,5	3,5,7, 28-36			0		0		ns

TABLE III B GROUP (A) TESTS - SUBGROUPS 9,10,11,7,8 (Concluded)

SYMBOL	TEST NUMBER	TEST PATTERN NUMBER	WAVEFORM FIGURE	MEASUREMENT TERMINALS				TEST LIMITS						UNITS
				DIP		FLATPACK		SUBGROUP 9 +25°C		SUBGROUP 10 +125°C		SUBGROUP 11 -55°C		
				INPUT UNDER TEST	OUTPUT UNDER TEST	INPUT UNDER TEST	OUTPUT UNDER TEST	MIN	MAX	MIN	MAX	MIN	MAX	
FUNCTIONAL TEST-MilStd 883 METHODS 3003,6,7,14		TABLE V	13	SUBGROUP (7):		TABLE V	VCC = 4.5V							
				SUBGROUP (7):		TABLE V	VCC = 5.5V							
				SUBGROUP (8):		TABLE V	REPEAT SUBGROUP 7 AT +125°C							
				SUBGROUP (8):		TABLE V	REPEAT SUBGROUP 7 AT -55°C							

NOTES:

1. Tests of subgroups 9,10 and 11 per MIL STD 883 Method 3003.
2. VCC = 4.5V and 5.5V for subgroups 9,10 and 11.
3. Where propagation delay tests for subgroups 9, 10 and 11 indicate a group of pins and where two or more propagation delays are specified for a test, only the reading for the pin with the worst case maximum delay requires recording.

APPENDIX B
TEST PROGRAMS AND DATA
FOR THE TEKTRONIX 3260
FOR THE 8212

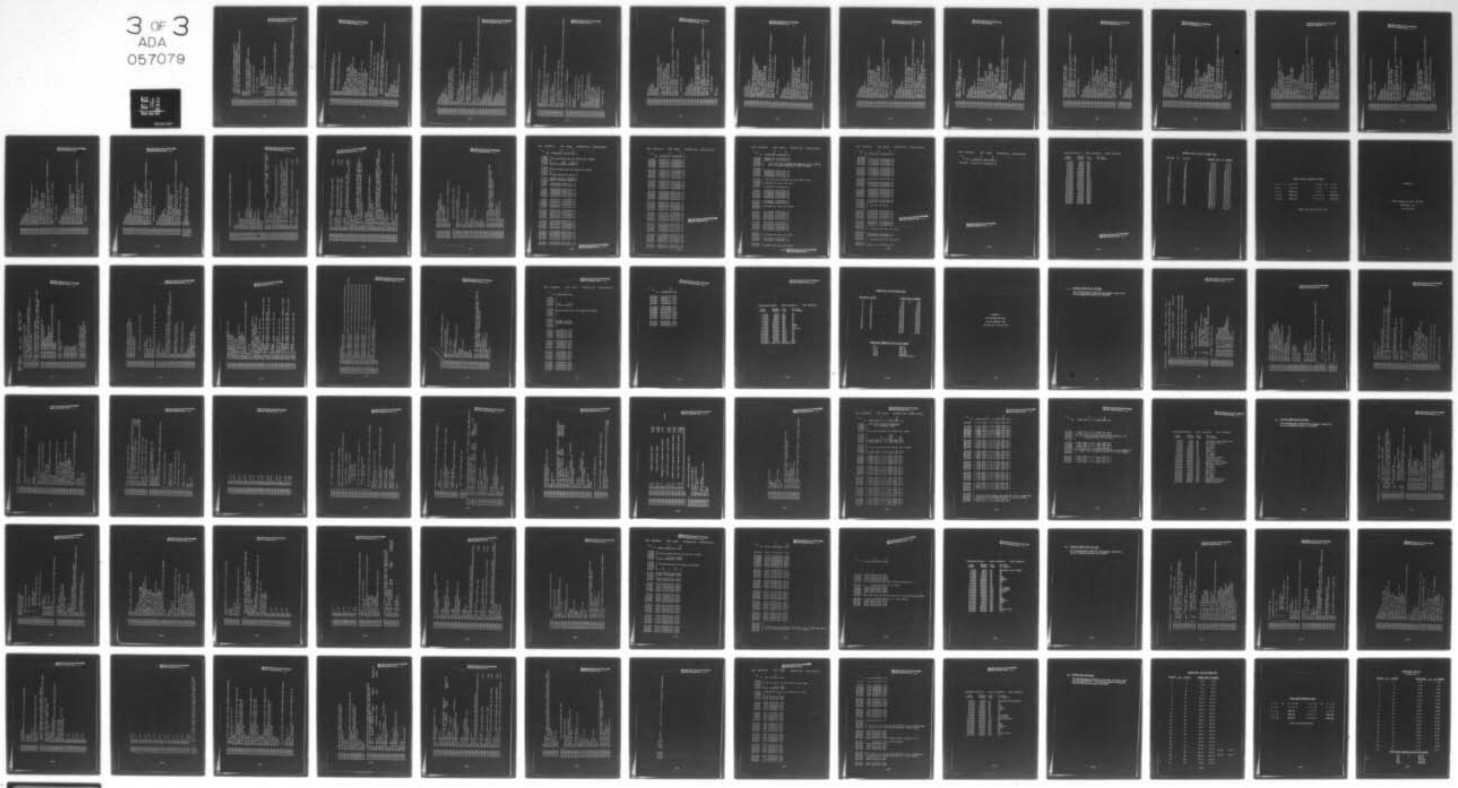
```
8212.FDT;WCT                                DISK NAME:  ETEC-12
DATE  07-FEB-78     TIME  10:52             PAGE   1 OF  13

1.0100 *          THIS TEST IS FOR THE 8212 DEVICE (EIGHT-BIT I/O PORT)
1.0200 *  WRITTEN BY L.W.ROLLER
1.0300 *  PAP TABLE USED WITH THIS TABLE IS 8212.PIN;LWR
1.0400 *  TEST PATTERN FILE NAME FOR THIS DEVICE IS P8212.PAT;LWR
1.0430 * THE SOCKET CARD IS S/N 2010
1.0500 *  LOAD 1 MODULES L1-C ARE REQUIRED ON SECTORS: 2,10,13,18,21,26,29,37,57
1.0600
1.0700 *         TABLE OF CONTENTS
1.0800 *  PART     DESCRIPTION OF CONTENTS
1.0900
1.1000 *    2      PINLISTS, ARRAYS, AND CONSTANTS
1.1100 *    3      FUNCTIONAL TESTS
1.1200 *    4      PROPAGATION DELAY TIME MEASUREMENTS
1.1300 *    5      PROPAGATION DELAY TIME MEASUREMENTS
1.1400 *   50      PASS/FAIL SORT ROUTINE, OUTPUT ROUTINE

2.0100    PINLIST DINS  = SP3,SP5,SP7,SP9,SP16,SP18,SP20,SP22
2.0200    PINLIST DOUTS = SP4,SP6,SP8,SP10,SP15,SP17,SP19,SP21
2.0300    PINLIST DS    = SP1,SP13
2.0400    PINLIST INS   = SP14,SP2,DS,SP11,DINS
2.0500    PINLIST OUTS  = DOUTS,SP23
2.0600    PINLIST ALL   = INS,OUTS
2.0700    PINLIST GND   = SP12
2.0800    PINLIST VCC   = SP24
2.0900    SUBROUTINE EVS6(0),DVS6(0),EVS7(0),DVS7(0):MC3
2.1000    FUNCTION MVS6(V),IVS6(0):MC3
2.1100    SUBROUTINE STRNGO(V,I,V,V),SCON(I,V,V,C):STRING
2.1200    SUBROUTINE CRDATE(V),CRTIME(V):TIME
2.1300    FUNCTION GETBIT(I,V,V,V):BARRAY
2.1400    SUBROUTINE BARRAY(I,V,V,V):BARRAY
2.1500    SUBROUTINE SREAD(P,V,V,V,V,I,V):SREAD
2.1600    IARRAY BER(100),PIN(10),C(75),D(75)
2.1700    ARRAY FF(75,10),V(75)
2.1800    BARRAY(BER,2,9,75)
```

AD-A057 079 GENERAL ELECTRIC CO PITTSFIELD MASS F/G 9/2
CHARACTERIZATION OF COMPLEX MICROPROCESSORS AND SUPPORT CHIPS.(U)
JUN 78 T M OSTROWSKI F30602-77-C-0012
UNCLASSIFIED RADC-TR-78-138 NL

3 OF 3
ADA
057079



END
DATE
FILMED
9-78
DDC

```
2.1900
2.2000 *     NUM(P) IS NUMBER OF MEASUREMENTS IN PARAMETER P
2.2100 *     P IS A NUMBER ASSIGNED TO EACH PARAMETER
2.2200 *    NP=21 IS NUMBER OF DIFFERENT PARAMETERS MEASURED
2.2300 *    MN=10 IS MAXIMUM NUMBER OF MEASUREMENTS OF ANY ONE PARAMETER
2.2400
2.2500    NP=23
2.2600    MN=10
2.2700    ARRAY VALUE(23,10), MAX(23), MIN(23)
2.2800    IARRAY NUM(23), NLESS(23), NGRE(23), NPASS(23)
2.2900    IARRAY PNAM(400),ST(23),SP(23)
2.3000
2.3100 *    ASSIGNMENTS ARE AS FOLLOWS
2.3200
2.3300 *    LUN   DATA OUTPUT
2.3400
2.3500 *      3       SELECTION QUERY
2.3600 *      4       TEST SUMMARY
2.3700 *      5       DATA ON A SPECIFIC PARAMETER
2.3750    PRINT <5> ERASE
2.3800    PRINT <5> CR,"DATE:"
2.3900    CRDATE(5)
2.4000    PRINT <5> CR,"TIME:"
2.4100    CRTIME(5)
2.4200    PRINT <5> CR,"THIS TEST IS FOR THE 8212 DEVICE",CR

3.0100    INITIALIZE
3.0200    VS6 = 5V AT 130MA
3.0300    EVS6
3.0310    WAIT 1S
3.0400    X = MVS6(10)
3.0500    Y = IVS6
3.0600    IF(5MA<Y<130MA) 3.11,3.11,3.07
3.0700    PRINT <4> "DEVICE DRAWS MORE THAN 130MA OF CURRENT"
3.0800    PRINT <4> CR,CR,"CHECK TO ENSURE DEVICE IS INSTALLED CORRECTLY",CR
3.0900    DVS6
3.1000    STOP
```

```
3.1100    IF(4.75V<X<5.25V)3.12,3.18,3.15
3.1200    PRINT <4> "SUPPLY VOLTAGE IS <4.75V",CR
3.1300    DVS6
3.1400    STOP
3.1500    PRINT <4> "SUPPLY VOLTAGE IS > 5.25V",CR
3.1600    DVS6
3.1700    STOP
3.1800    CONTINUE
3.1900    CYCLE = 500NS
3.2000    HICOMPARE = 200NS FOR 100NS
3.2100    LOCOMPARE = 200NS FOR 100NS
3.2200    CONNECT INPUT TO DRIVER ON INS
3.2300    CONNECT OUTPUT TO COMPARATOR ON OUTS
3.2400    HICOMPARE = 3.65V ON OUTS
3.2500    LOCOMPARE = 0.45V ON OUTS
3.2600    HIDRIVE = 2.0V ON INS
3.2700    LODRIVE = 0.85V ON INS
3.2800    LOAD DISK P8212 TO ALL WITH FI,CM
3.2900    FORCE INS WITH PATTERN
3.3000    COMPARE OUTS WITH PATTERN
3.3100    MASK OUTS WITH PATTERN
3.3200
3.3300    MOVE REGISTER (77) TO ALL WITH FI,CM AND SAVE ERRORS
3.3500    IF (ERROR) 60.03
3.3600    PRINT <4> "PASSED FUNCTIONAL TEST ",CR
3.3700    CONTINUE
3.3800    DISCONNECT OUTPUT FROM COMPARATOR ON OUTS
3.3900 *
3.4000 *     CHECK FUNCTION OF DISABLING OUTPUTS
3.4100 *   MEASURE OUTPUT LEAKAGE CURRENT WITH OUTPUTS IN HIGH IMPEDANCE STATE
3.4200 *
3.4250    LOAD DISK P8212 TO ALL WITH FI,CM
3.4300    P=20
3.4400    NUM(P)=8
3.4500    MIN(P)=-20UA
3.4600    MAX(P)=20UA
3.4700    ST(P)=1+(P-1)*16
3.4800    SP(P)=P*16
3.4900    SCON(PNAM,ST(P),SP(P),"IOFF(L)")
```

```
3.5000   P=P+1
3.5100   NUM(P)=8
3.5200   MIN(P)=-20UA
3.5300   MAX(P)=20UA
3.5400   ST(P)=1+(P-1)*16
3.5500   SP(P)=P*16
3.5600   SCON(PNAM,ST(P),SP(P),"IOFF(H)")
3.5650   LOAD DISK PB212 TO ALL WITH FI,CM
3.5700   MOVE REGISTER (67) TO ALL WITH FI,CM
3.5800   Y=0
3.5900   P=20
3.6000   LOOP 3.69 I=1,8
3.6100   SETUP TO MEASURE CURRENT ON DOUTS(I) FROM VS4=0.45V AT 30UA
3.6200   VALUE(P,I) = CURRENT
3.6300   IF (-20UA<VALUE(P,I)<20UA) 3.65
3.6400   Y=1
3.6500   VS4 =5.25V AT 30UA
3.6600   VALUE(P+1,I) = CURRENT
3.6700   IF (-20UA<VALUE(P+1,I)<20UA) 3.69
3.6800   Y=1
3.6900   UNSET TO MEASURE CURRENT ON DOUTS(I) FROM VS4
3.7000   IF (Y EQ 0) 3.72
3.7100   PRINT <4> "FAILED OUTPUT LEAKAGE CURRENT TEST WHICH IS PART OF FUNCTIONAL TESTS",CR
3.7200   CONTINUE
3.8000   P=22
3.8010   NUM(P)=8
3.8020   MIN(P)=-20UA
3.8030   MAX(P)=20UA
3.8040   ST(P)=1+(P-1)*16
3.8050   SP(P)=P*16
3.8060   SCON(PNAM,ST(P),SP(P),"IOFF(L)")
3.8070   P=P+1
3.8080   NUM(P)=8
3.8090   MIN(P)=-20UA
3.8100   MAX(P)=20UA
3.8110   ST(P)=1+(P-1)*16
3.8120   SP(P)=P*16
3.8130   SCON(PNAM,ST(P),SP(P),"IOFF(H)")
3.8140   LOAD DISK PB212 TO ALL WITH FI,CM
```

```
3.8150   MOVE REGISTER (70) TO ALL WITH FI,CM
3.8170   P=22
3.8180   LOOP 3.827 I=1,A
3.8190   SETUP TO MEASURE CURRENT ON DOUTS(I) FROM VS4=0.45V AT 30UA
3.8200   VALUE(P,I) = CURRENT
3.8210   IF (-20UA<VALUE(P,I)<20UA) 3.823
3.8220   Y=1
3.8230   VS4 =5.25V AT 30UA
3.8240   VALUE(P+1,I) = CURRENT
3.8250   IF (-20UA<VALUE(P+1,I)<20UA) 3.827
3.8260   Y=1
3.8270   UNSET TO MEASURE CURRENT ON DOUTS(I) FROM VS4
3.8280   IF (Y EQ 0) 3.83
3.8290   PRINT <4> CR,"FAILED OUTPUT LEAKAGE CURRENT TEST WHICH IS PART OF FUNCTIONAL TESTS",CR
3.8300   CONTINUE

4.0010 *  PROPAGATION DELAY TIME MEASUREMENTS
4.0020
4.0030 *  TIMING SETUP
4.0040
4.0050   CYCLE=1US
4.0060   DATAPHASE FROM 100NS FOR 500NS
4.0070
4.0080 *          PROGRAM CONNECTIONS
4.0090
4.0100   CONNECT OUTPUT TO LOAD1 ON OUTS
4.0102   FVS7
4.0103   VS7=2.1V AT 280MA
4.0110   CONNECT INPUT TO DRIVER ON INS
4.0120   CONNECT OUTPUT TO COMPARATOR ON ALL
4.0130   HIDRIVE=4.5V ON INS
4.0140   HIDRIVE=3.0V ON DINS
4.0150   HIDRIVE=3.0V ON SP11
4.0160   LODRIVE=0V ON INS
4.0170   LOCOMPARE=1.5V ON ALL
4.0180   HICOMPARE=1.5V ON ALL
4.0190
4.0200 *     TESTS FOR TPHL1
4.0210
```

```
4.0220    P=1
4.0230    NUM(P)=8
4.0240    MIN(P)=0NS
4.0250    MAX(P)=30NS
4.0260    ST(P)=1
4.0270    SP(P)=16
4.0280    SCON(PNAM,ST(P),SP(P),"TPHL1 (DI-DO)")
4.0290 *          LOAD DATA FOR INPUTS
4.0300    LOAD DISK PA212 (77,129) TO INS
4.0310    FORCE INS WITH PATTERN
4.0320    FORCE DINS WITH PATTERN;RZ
4.0330    LOCOMPARE FROM 400NS FOR 400NS
4.0340    HICOMPARE FROM 400NS FOR 400NS
4.0350    LOOP 4.039 I=1,8
4.0360    SETUP TO MEASURE TIME ON DINS(I)- TO DOUTS(I)- AT 30NS,TRIGGER 2
4.0370    MOVE FROM REGISTER (I,I+1) TO INS
4.0380    VALUE(P,I)=TIME
4.0390    UNSET TO MEASURE TIME ON DINS(I) TO DOUTS(I)
4.0400
4.0410 *     TESTS FOR TPLH1
4.0420
4.0430    P=7
4.0440    NUM(P)=8
4.0450    MIN(P)=0NS
4.0460    MAX(P)=42NS
4.0470    ST(P)=1+(P-1)*16
4.0480    SP(P)=P*16
4.0490    SCON(PNAM,ST(P),SP(P),"TPLH1 (DI-DO)")
4.0500    LOCOMPARE FROM 50NS FOR 300NS
4.0510    HICOMPARE FROM 50NS FOR 300NS
4.0520    LOOP 4.056 I=1,8
4.0530    SETUP TO MEASURE TIME ON DINS(I)+ TO DOUTS(I)+ AT 42NS,TRIGGER 2
4.0540    MOVE FROM REGISTER (I,I+1) TO INS
4.0550    VALUE(P,I)=TIME
4.0560    UNSET TO MEASURE TIME ON DINS(I) TO DOUTS(I)
4.0570
4.0580 *     TESTS FOR TPHL2
4.0590
4.0600    P=2
4.0610    NUM(P)=8
```

```
4.0620    MIN(P)=0NS
4.0630    MAX(P)=37NS
4.0640    ST(P)=1+(P-1)*16
4.0650    SP(P)=P*16
4.0660    SCON(PNAM,ST(P),SP(P),"TPHL2 (STB-DO)")
4.0670    FORCE DINS WITH PATTERN;RZ,INVERT
4.0680    DATAPHASE FROM 100NS FOR 200NS
4.0690    PHASE3 FROM 150NS FOR 30NS
4.0700    FORCE SP11 WITH PATTERN;RZ
4.0710    CONNECT TO PHASE ON SP11
4.0720    LOCOMPARE FROM 150NS FOR 200NS
4.0730    HICOMPARE FROM 150NS FOR 200NS
4.0740    LOOP 4.078 I=1,8
4.0750    SETUP TO MEASURE TIME ON SP11+ TO DOUTS(I)- AT 37NS,TRIGGER 2
4.0760    MOVE FROM REGISTER (9+I,10+I) TO INS
4.0770    VALUE(P,I)=TIME
4.0780    UNSET TO MEASURE TIME ON SP11 TO DOUTS(I)
4.0790
4.0800 *     TESTS FOR TPLH2
4.0810
4.0820    P=8
4.0830    NUM(P)=8
4.0840    MIN(P)=0NS
4.0850    MAX(P)=55NS
4.0860    ST(P)=1+(P-1)*16
4.0870    SP(P)=P*16
4.0880    SCON(PNAM,ST(P),SP(P),"TPLH2 (STB-DO)")
4.0890    DATAPHASE FROM 500NS FOR 200NS
4.0900    PHASE3 FROM 600NS FOR 30NS
4.0910    LOCOMPARE FROM 550NS FOR 200NS
4.0920    HICOMPARE FROM 550NS FOR 200NS
4.0930    LOOP 4.097 I=1,8
4.0940    SETUP TO MEASURE TIME ON SP11+ TO DOUTS(I)+ AT 55NS,TRIGGER 2
4.0950    MOVE FROM REGISTER (10+I,11+I) TO INS
4.0960    VALUE(P,I)=TIME
4.0970    UNSET TO MEASURE TIME ON SP11 TO DOUTS(I)
4.0980
4.0990 *     TESTS FOR TPHL3
4.1000
```

```
4.1010    P=3
4.1020    NUM(P)=1
4.1030    MIN(P)=0NS
4.1040    MAX(P)=37NS
4.1050    ST(P)=1+(P-1)*16
4.1060    SP(P)=P*16
4.1070    SCON(PNAM,ST(P),SP(P),"TPHL3 (ST8-INT)")
4.1080    DATAPHASE = 100NS FOR 30NS
4.1090    FORCE SP13 WITH PATTERN;RZ
4.1100    PHASE3 FROM 300NS FOR 30NS
4.1110    CONNECT TO PHASE ON SP11
4.1120    LOCOMPARE FROM 315NS FOR 300NS
4.1130    HICOMPARE FROM 315NS FOR 300NS
4.1140    LOOP 4.118 I=1,8
4.1150    SETUP TO MEASURE TIME ON SP11- TO SP23- AT 37NS,TRIGGER 2
4.1160    MOVE FROM REGISTER (19,20) TO INS
4.1170    VALUE(P,I)=TIME
4.1180    UNSET TO MEASURE TIME ON SP11 TO SP23
4.1190
4.1200 *     TESTS FOR TPLH3
4.1210
4.1220    P=9
4.1230    NUM(P)=2
4.1240    MIN(P)=0NS
4.1250    MAX(P)=55NS
4.1260    ST(P)=1+(P-1)*16
4.1270    SP(P)=P*16
4.1280    SCON(PNAM,ST(P),SP(P),"TPLH3 (DS2-INT)")
4.1290    LOCOMPARE FROM 515NS FOR 300NS
4.1300    HICOMPARE FROM 515NS FOR 300NS
4.1310    DATAPHASE FROM 500NS FOR 30NS
4.1320    SETUP TO MEASURE TIME ON SP13- TO SP23+ AT 55NS,TRIGGER 2
4.1330    MOVE FROM REGISTER (19,20) TO INS
4.1340    VALUE(P,1)=TIME
4.1350    UNSET TO MEASURE TIME ON SP13 TO SP23
4.1360    FORCE SP13 WITH PATTERN
4.1370    FORCE SP1 WITH PATTERN;RZ,INVERT
4.1380    SETUP TO MEASURE TIME ON SP1+ TO SP23+ AT 55NS,TRIGGER 2
4.1390    MOVE REGISTER (20,21) TO INS
```

```
4.1400    VALUE (P,2)=TIME
4.1410    UNSET TO MEASURE TIME ON SP1 TO SP23
4.1420    CONNECT TO DATAPHASE ON SP11
4.1430
4.1440 *     TESTS FOR TPHL4
4.1450
4.1460    P=4
4.1470    NUM(P)=8
4.1480    MIN(P)=0NS
4.1490    MAX(P)=37NS
4.1500    ST(P)=1+(P-1)*16
4.1510    SP(P)=P*16
4.1520    SCON(PNAM,ST(P),SP(P),"TPHL4 (DS1-DO)")
4.1530    HIDRIVE=4.5V ON INS
4.1540    HIDRIVE=3.0V ON DINS
4.1550    HIDRIVE=3.0V ON SP1
4.1560    DATAPHASE =100NS FOR 200NS
4.1570    FORCE INS WITH PATTERN
4.1580    FORCE DINS WITH PATTERN;RZ, INVERT
4.1590    FORCE SP1 WITH PATTERN;RZ, INVERT
4.1600    PHASE1 FROM 150NS FOR 30NS
4.1610    CONNECT TO PHASE ON SP1
4.1620    LOCOMPARE FROM 125NS FOR 400NS
4.1630    HICOMPARE FROM 125NS FOR 400NS
4.1640    LOOP 4.168 I=1,8
4.1650    SETUP TO MEASURE TIME ON SP1- TO DOUTS(I)- AT 37NS,TRIGGER 2
4.1660    MOVE FROM REGISTER (21+I,22+I) TO INS
4.1670    VALUE(P,I)=TIME
4.1680    UNSET TO MEASURE TIME ON SP1 TO DOUTS(I)
4.1690
4.1700 *     TESTS FOR TPLH4
4.1710
4.1720    P=10
4.1730    NUM(P)=8
4.1740    MIN(P)=0NS
4.1750    MAX(P)=50NS
4.1760    ST(P)=1+(P-1)*16
4.1770    SP(P)=P*16
4.1780    SCON(PNAM,ST(P),SP(P),"TPLH4 (DS1-DO)")
```

```
4.1790    LOCOMPARE FROM 125NS FOR 400NS
4.1800    HICOMPARE FROM 125NS FOR 400NS
4.1810    LOOP 4,185 I=1,8
4.1820    SETUP TO MEASURE TIME ON SP1- TO DOUTS(I)+ AT 50NS,TRIGGER 2
4.1830    MOVE FROM REGISTER (22+I,23+I) TO INS
4.1840    VALUE(P,I)=TIME
4.1850    UNSET TO MEASURE TIME ON SP1 TO DOUTS(I)
4.1860
4.1870 *     TESTS FOR TPHL4
4.1880
4.1890    P=5
4.1900    NUM(P)=8
4.1910    MIN(P)=0NS
4.1920    MAX(P)=37NS
4.1930    ST(P)=1+(P-1)*16
4.1940    SP(P)=P*16
4.1950    SCON(PNAM,ST(P),SP(P),"TPHL4 (DS2-DO)")
4.1960    HIDRIVE=3.0V ON SP13
4.1970    FORCE SP13 WITH PATTERN;RZ
4.1980    CONNECT TO DATAPHASE ON SP1
4.1990    FORCE SP1 WITH PATTERN
4.2000    PHASE4 FROM 150NS FOR 30NS
4.2010    CONNECT TO PHASE ON SP13
4.2020    LOCOMPARE FROM 125NS FOR 300NS
4.2030    HICOMPARE FROM 125NS FOR 300NS
4.2040    LOOP 4,208 I=1,8
4.2050    SETUP TO MEASURE TIME ON SP13+ TO DOUTS(I)- AT 37NS,TRIGGER 2
4.2060    MOVE FROM REGISTER (31+I,32+I) TO INS
4.2070    VALUE(P,I)=TIME
4.2080    UNSET TO MEASURE TIME ON SP13 TO DOUTS(I)

5.0010
5.0020 *     TESTS FOR TPLH4
5.0030
5.0040    P=11
5.0050    NUM(P)=8
5.0060    MIN(P)=0NS
5.0070    MAX(P)=50NS
5.0080    ST(P)=1+(P-1)*16
```

```
5.0090    SP(P)=P*16
5.0100    SCON(PNAM,ST(P),SP(P),"TPLH4 (DS2-DO)")
5.0110    LOCOMPARE FROM 125NS FOR 300NS
5.0120    HICOMPARE FROM 125NS FOR 300NS
5.0130    LOOP 5.017 I=1,8
5.0140    SETUP TO MEASURE TIME ON SP13+ TO DOUTS(I)+ AT 50NS,TRIGGER 2
5.0150    MOVE FROM REGISTER (32+I,33+I) TO INS
5.0160    VALUE(P,I)=TIME
5.0170    UNSET TO MEASURE TIME ON SP13 TO DOUTS(I)
5.0180
5.0190 *     TESTS FOR TPHL5
5.0200
5.0210    P=6
5.0220    NUM(P)=8
5.0230    MIN(P)=0NS
5.0240    MAX(P)=60NS
5.0250    ST(P)=1+(P-1)*16
5.0260    SP(P)=P*16
5.0270    SCON(PNAM,ST(P),SP(P),"TPHL5 (CLR-DO)")
5.0280    PHASE4 FROM 100NS FOR 200NS
5.0290    HIDRIVE=4.5V ON INS
5.0300    HIDRIVE=3.0V ON SP13
5.0310    HIDRIVE=3.0V ON SP14
5.0320    DATAPHASE=200NS FOR 30NS
5.0330    FORCE INS WITH PATTERN
5.0340    FORCE SP13 WITH PATTERN;RZ,INVERT
5.0350    FORCE SP14 WITH PATTERN;RZ,INVERT
5.0360    LOCOMPARE FROM 150NS FOR 300NS
5.0370    HICOMPARE FROM 150NS FOR 300NS
5.0380    LOOP 5.042 I=1,8
5.0390    SETUP TO MEASURE TIME ON SP14- TO DOUTS(I)- AT 60NS,TRIGGER 2
5.0400    MOVE FROM REGISTER (40+I,41+I) TO INS
5.0410    VALUE(P,I)=TIME
5.0420    UNSET TO MEASURE TIME ON SP14 TO DOUTS(I)
5.0430
5.0440 *     TESTS FOR TPZL1
5.0450
5.0460    P=12
5.0470    NUM(P)=8
```

```
5.0480    MIN(P)=0NS
5.0490    MAX(P)=50NS
5.0500    ST(P)=1+(P-1)*16
5.0510    SP(P)=P*16
5.0520    SCON(PNAM,ST(P),SP(P),"TPZL1 (DS1-D0)")
5.0530    CONNECT TO DATAPHASE ON SP13
5.0540    DATAPHASE=100NS FOR 500NS
5.0550    LOCOMPARE=1.5V ON INS
5.0560    HICOMPARE=1.5V ON INS
5.0570    LOCOMPARE=1.0V ON OUTS
5.0580    HICOMPARE=1.0V ON OUTS
5.0590    LOCOMPARE FROM 500NS FOR 300NS
5.0600    HICOMPARE FROM 500NS FOR 300NS
5.0610    HIDRIVE=4.5V ON INS
5.0620    HIDRIVE=3.0V ON SP1
5.0630    LODRIVE=0V ON INS
5.0640    FORCE INS WITH PATTERN
5.0650    FORCE SP1 WITH PATTERN;RZ
5.0660    FORCE SP13 WITH PATTERN;RZ,INVERT
5.0670    LOOP 5.071 I=1,8
5.0680    SETUP TO MEASURE TIME ON SP1- TO DOUTS(I)- AT 50NS,TRIGGER 2
5.0690    MOVE FROM REGISTER (49,50) TO INS
5.0700    VALUE(P,I)=TIME
5.0710    UNSET TO MEASURE TIME ON SP1 TO DOUTS(I)
5.0720
5.0730 *     TESTS FOR TPLZ1
5.0740
5.0750    P=16
5.0760    NUM(P)=8
5.0770    MIN(P)=0NS
5.0780    MAX(P)=50NS
5.0790    ST(P)=1+(P-1)*16
5.0800    SP(P)=P*16
5.0810    SCON(PNAM,ST(P),SP(P),"TPLZ1 (DS1-D0)")
5.0820    LOCOMPARE FROM 50NS FOR 300NS
5.0830    HICOMPARE FROM 50NS FOR 300NS
5.0840    LOOP 5.088 I=1,8
5.0850    SETUP TO MEASURE TIME ON SP1+ TO DOUTS(I)+ AT 50NS,TRIGGER 2
5.0860    MOVE FROM REGISTER (49,50) TO INS
```

```
5.0870    VALUE(P,I)=TIME
5.0880    UNSET TO MEASURE TIME ON SP1 TO DOUTS(I)
5.0890
5.0900 *    TESTS FOR TPZL1
5.0910
5.0920    P=13
5.0930    NUM(P)=8
5.0940    MIN(P)=0NS
5.0950    MAX(P)=50NS
5.0960    ST(P)=1+(P-1)*16
5.0970    SP(P)=P*16
5.0980    SCON(PNAM,ST(P),SP(P),"TPZL1 (DS2-DO)")
5.0990    LOCOMPARE FROM 500NS FOR 300NS
5.1000    HICOMPARE FROM 500NS FOR 300NS
5.1010    LOOP 5.105 I=1,8
5.1020    SETUP TO MEASURE TIME ON SP13+ TO DOUTS(I)- AT 50NS,TRIGGER 2
5.1030    MOVE FROM REGISTER (50,51) TO INS
5.1040    VALUE(P,I)=TIME
5.1050    UNSET TO MEASURE TIME ON SP13 TO DOUTS(I)
5.1060
5.1070 *    TESTS FOR TPLZ1
5.1080
5.1090    P=17
5.1100    NUM(P)=8
5.1110    MIN(P)=0NS
5.1120    MAX(P)=50NS
5.1130    ST(P)=1+(P-1)*16
5.1140    SP(P)=P*16
5.1150    SCON(PNAM,ST(P),SP(P),"TPLZ1 (DS2-DO)")
5.1160    LOCOMPARE FROM 50NS FOR 300NS
5.1170    HICOMPARE FROM 50NS FOR 300NS
5.1180    LOOP 5.122 I=1,8
5.1190    SETUP TO MEASURE TIME ON SP13- TO DOUTS(I)+ AT 50NS,TRIGGER 2
5.1200    MOVE FROM REGISTER (50,51) TO INS
5.1210    VALUE(P,I)=TIME
5.1220    UNSET TO MEASURE TIME ON SP13 TO DOUTS(I)
5.1230
5.1240 *    TESTS FOR TPZH1
5.1250
```

```
5.1260    P=14
5.1270    NUM(P)=8
5.1280    MIN(P)=0NS
5.1290    MAX(P)=50NS
5.1300    ST(P)=1+(P-1)*16
5.1310    SP(P)=P*16
5.1320    SCON(PNAM,ST(P),SP(P),"TPZH1 (DS1-DO)")
5.1330    HIDRIVE=4.5V ON SP13
5.1340    FORCE SP1 WITH PATTERN;RZ
5.1350    FORCE SP13 WITH PATTERN;RZ,INVERT
5.1360    LOCOMPARE=2.6V ON OUTS
5.1370    HICOMPARE=2.6V ON OUTS
5.1380    LOCOMPARE FROM 500NS FOR 300NS
5.1390    HICOMPARE FROM 500NS FOR 300NS
5.1400    LOOP 5.144 I=1,8
5.1410    SETUP TO MEASURE TIME ON SP1- TO DOUTS(I)+ AT 50NS,TRIGGER 2
5.1420    MOVE FROM REGISTER (51,52) TO INS
5.1430    VALUE(P,I)=TIME
5.1440    UNSET TO MEASURE TIME ON SP1 TO DOUTS(I)
5.1450
5.1460 *     TESTS FOR TPHZ1
5.1470
5.1480    P=18
5.1490    NUM(P)=8
5.1500    MIN(P)=0NS
5.1510    MAX(P)=150NS
5.1520    ST(P)=1+(P-1)*16
5.1530    SP(P)=P*16
5.1540    SCON(PNAM,ST(P),SP(P),"TPHZ1 (DS1-DO)")
5.1550    LOCOMPARE FROM 50NS FOR 300NS
5.1560    HICOMPARE FROM 50NS FOR 300NS
5.1570    LOOP 5.161 I=1,8
5.1580    SETUP TO MEASURE TIME ON SP1+ TO DOUTS(I)- AT 150NS,TRIGGER 2
5.1590    MOVE FROM REGISTER (51,52) TO INS
5.1600    VALUE(P,I)=TIME
5.1610    UNSET TO MEASURE TIME ON SP1 TO DOUTS(I)
5.1620
5.1630 *     TESTS FOR TPZH1
5.1640
```

```
5.1650    P=15
5.1660    NUM(P)=8
5.1670    MIN(P)=0NS
5.1680    MAX(P)=50NS
5.1690    ST(P)=1+(P-1)*16
5.1700    SP(P)=P*16
5.1710    SCON(PNAM,ST(P),SP(P),"TPZH1 (DS2-DO)")
5.1720    HIDRIVE=3.0V ON SP13
5.1730    FORCE SP13 WITH PATTERN;RZ,INVERT
5.1740    LOCOMPARE FROM 500NS FOR 300NS
5.1750    HICOMPARE FROM 500NS FOR 300NS
5.1760    LOOP 5.18 I=1,8
5.1770    SETUP TO MEASURE TIME ON SP13+ TO DOUTS(I)+ AT 50NS,TRIGGER 2
5.1780    MOVE FROM REGISTER (52,53) TO INS
5.1790    VALUE(P,I)=TIME
5.1800    UNSET TO MEASURE TIME ON SP13 TO DOUTS(I)
5.1810
5.1820 *     TESTS FOR TPHZ1
5.1830
5.1840    P=19
5.1850    NUM(P)=8
5.1860    MIN(P)=0NS
5.1870    MAX(P)=150NS
5.1880    ST(P)=1+(P-1)*16
5.1890    SP(P)=P*16
5.1900    SCON(PNAM,ST(P),SP(P),"TPHZ1 (DS2-DO)")
5.1910    LOCOMPARE FROM 50NS FOR 300NS
5.1920    HICOMPARE FROM 50NS FOR 300NS
5.1930    LOOP 5.197 I=1,8
5.1940    SETUP TO MEASURE TIME ON SP13- TO DOUTS(I)- AT 150NS,TRIGGER 2
5.1950    MOVE FROM REGISTER (52,53) TO INS
5.1960    VALUE(P,I)=TIME
5.1970    UNSET TO MEASURE TIME ON SP13 TO DOUTS(I)

50.0001   DVS7
50.0010   DISCONNECT OUTPUT FROM LOAD1 ON OUTS
50.0100   DISCONNECT INPUT FROM DRIVER ON INS
50.0200   DVS6
50.0300
```

```
50.0400 *     THE FOLLOWING IS USED TO SORT PASSED/FAILED TESTS
50.0500
50.0600
50.0700     TOT=0
50.0800     FA=0
50.0900     LOOP 50.12 I=1,NP
50.1000     NLESS(I)=0
50.1100     NPASS(I)=0
50.1200     NGRE(I)=0
50.1300     LOOP 50.22 P=1,NP
50.1400     LOOP 50.21 I=1,NUM(P)
50.1500     IF (MIN(P)<VALUE(P,I)<MAX(P)) 50.16,50.2,50.18
50.1600     NLESS(P)=NLESS(P)+1
50.1700     GOTO 50.21
50.1800     NGRE(P)=NGRE(P)+1
50.1900     GOTO 50.21
50.2000     NPASS(P)=NPASS(P)+1
50.2100     CONTINUE
50.2200     CONTINUE
50.2300
50.2400     PRINT <4> CR,CR,CR,"          COMPILED PARAMETRIC TEST RESULTS",CR,CR,CR
50.2500     PRINT <4> "          PARAMETER       #MEASURED   #PASSED    #<MIN    #>MAX"
50.2600     PRINT <4> CR,CR
50.2700     LOOP 50.32 P=1,NP
50.2800     PRINT <4> P:I2
50.2900     STRNGO(4,PNAM,ST(P),SP(P))
50.3000     PRINT <4> NUM(P):I,"     ",NPASS(P):I,NLESS(P):I,NGRE(P):I,CR
50.3100     TOT=TOT+NUM(P)
50.3200     FA=FA+NLESS(P)+NGRE(P)
50.3300     PRINT <4> CR,"  TOTAL NUMBER OF PARAMETRIC  FAILURES = ",FA:I,CR
50.3400     PRINT <4> "  TOTAL NUMBER OF PARAMETRIC TESTS = ",TOT:I,CR
50.3402     PRINT <4> CR,CR,CR,"SUMMARY OF ALL TEST RESULTS",CR,CR
50.3404     PRINT <4> "*************************************************",CR
50.3406     S=0
50.3408     IF (A EQ 0) 50.3416
50.3410     PRINT <4> "*  FAILED ",A:I," OUT OF 73 FUNCTIONAL TESTS     *",CR
50.3412     S=1
50.3414     GOTO 50.3418
50.3416     PRINT <4> "*  PASSED FUNCTIONAL TESTS                       *",CR
```

```
50.3418   IF (Y EQ 0) 50.3426
50.3420   PRINT <4> "*  FAILED OUTPUT LEAKAGE CURRENT TESTS              *",CR
50.3422   S=1
50.3424   GOTO 50.3428
50.3426   PRINT <4> "*  PASSED OUTPUT LEAKAGE CURRENT TESTS              *",CR
50.3428   IF (FA EQ 0) 50.3436
50.3430   PRINT <4> "*  FAILED PROPAGATION DELAY TIME TESTS              *",CR
50.3432   S=1
50.3434   GOTO 50.3438
50.3436   PRINT <4> "*  PASSED ALL PROPAGATION DELAY TIME TESTS          *",CR
50.3438   PRINT <4> "*************************************************",CR
50.3440   IF (S EQ 0) 50.3446
50.3442   DISPLAY 00,FAIL
50.3444   GOTO 50.35
50.3446   DISPLAY 00,PASS
50.3500   PRINT <3> CR,CR," IF YOU DESIRE A PRINTOUT OF SPECIFIC DATA",CR
50.3600   PRINT <3> "  TYPE ITS PARAMETER NUMBER DEFINED IN THE TEST PROGRAM,"
50.3700   PRINT <3> CR,"OR IF DATA ON ALL PARAMETERS IS DESIRED TYPE 99,"
50.3800   PRINT <3> " OTHERWISE TYPE 0    "
50.3900   ACCEPT P
50.4000   IF (P EQ 0) 50.65
50.4100   IF (P GT NP) 50.57
50.4200   PC=(NLESS(P)+NGRE(P))*100/(NLESS(P)+NGRE(P)+NPASS(P))
50.4300   PRINT <5> CR,CR,CR, " DATA ON "
50.4400   STRNGO(5,PNAM,ST(P),SP(P))
50.4500   PRINT <5> CR
50.4600   PRINT <5> " PER CENT OF READINGS WHICH FAIL THIS PARAMETER = ",PC,CR
50.4700   PRINT <5> "LIMITS FOR THIS PARAMETER ARE:  MIN=",MIN(P), "MAX=",MAX(P),CR,CR
50.4800   PRINT <5> "ACTUAL READINGS ON THIS PARAMETER ARE : ",CR,CR
50.4900   LOOP 50.54 I=1,NUM(P)
50.5000   PRINT <5> VALUE(P,I)
50.5100   J=INT(I/5)*5
50.5200   IF (J LT I) 50.54
50.5300   PRINT <5>  CR
50.5400   CONTINUE
50.5500   PRINT <3> CR,CR,CR," IF YOU DESIRE A PRINTOUT OF ANOTHER SET OF DATA ",CR
50.5600   GOTO 50.36
50.5700   PRINT <5> CR,CR,"   PARAMETER  :   LIMITS ",CR,"DATA "
50.5800   LOOP 50.64 I=1,NP
```

```
50.5900    PRINT <5> CR,CR
50.6000    STRNGO(5,PNAM,ST(I),SP(I))
50.6100    PRINT <5> " : ",MIN(I),MAX(I),CR
50.6200    LOOP 50.63 J=1,NUM(I)
50.6300    PRINT <5> VALUE(I,J)
50.6400    CONTINUE
50.6500    PRINT <3> CR,CR,CR,"  TEST IS COMPLETED",CR
50.6600    STOP

60.0100 *          SORT FAILING FUNCTIONAL TESTS
60.0200 *
60.0300    SREAD (OUTS,1,9,5,73,BER,2)
60.0400    PRESET PIN(1) = 4,6,8,10,15,17,19,21,23
60.0500    A=1
60.0600    LOOP 60.17 J=1,73
60.0700    S=0
60.0800    LOOP 60.12 I=1,9
60.0900    IF (NOT GETBIT(BER,1,I,J)) 60.12
60.1000    S=S+1
60.1100    FF(A,S)=I
60.1200    CONTINUE
60.1300    IF (S EQ 0) 60.17
60.1400    C(A)=J
60.1500    D(A)=S
60.1600    A=A+1
60.1700    CONTINUE
60.1800    A=A-1
60.1900
60.1950    PRINT <5> CR,CR
60.2000    PRINT <5> "FAILED ",A:I," OUT OF 73 FUNCTIONAL TESTS",CR,CR
60.2100    PRINT <5> "THE FOLLOWING FUNCTIONAL TESTS FAILED ",CR
60.2200    PRINT <5> "VECTOR NUMBER :  FAILING PINS",CR
60.2300    LOOP 60.27 J=1,A
60.2400    PRINT <5> CR,C(J):I,":  "
60.2500    LOOP 60.26 I=1,D(J)
60.2600    PRINT <5> PIN(FF(J,I)):I3
60.2700    CONTINUE
60.2800    GOTO 3.37
```

```
DATE  06-FEB-78      TIME  20:48      PATTERN FILE   P8212.PAT;WCT

  1                    0          0
    TO                 1          2
       22  1234567890 1234567890 12

  0.0001  *
  0.0002  * THE FOLLOWING ARE THE DEVICE PIN NUMBERS
  0.0003  *
  0.0004  *1  11      1122     11112 2
  0.0005  *42131 35796802 46805791 3

  0.0006  *
  0.0007  *THE FOLLOWING ARE THE DEVICE PIN NAMES
  0.0008  *
  0.0009  *- -                       -
  0.0010  *C DDS DDDDDDDD DDDDDDDD I

  0.0011  *LMSST IIIIIIII OOOOOOOO N
  0.0012  *RD12B 12345678 1234567A T
  0.0013  *
  1.0000   0100000000 000LLLLLLL LH
  2.0000   0101000000 000LLLLLLL LL

  3.0000   0001000000 000LLLLLLL LL
  4.0000   1001000000 000LLLLLLL LL
  5.0000   1101000000 000LLLLLLL LL
  6.0000   1100000000 000LLLLLLL LH
  7.0000   1100011111 111LLLLLLL LH

  8.0000   1101011111 111HHHHHHH HL
  9.0000   1100011111 111HHHHHHH HH
 10.0000   1101011111 111HHHHHHH HL
 11.0000   0101011111 111HHHHHHH HL
 12.0000   0001011111 111LLLLLLL LL

 13.0000   0001111111 111HHHHHHH HL
 14.0000   0001100000 000LLLLLLL LL
 15.0000   0001111111 111HHHHHHH HL
 16.0000   1001111111 111HHHHHHH HL
 17.0000   1001011111 111HHHHHHH HL

 18.0000   1001000000 000HHHHHHH HL
 19.0000   1001100000 000LLLLLLL LL
 20.0000   1001111111 111HHHHHHH HL
 21.0000   1001011111 111HHHHHHH HL
 22.0000   1001000000 000HHHHHHH HL

 23.0000   0001000000 000LLLLLLL LL
 24.0000   0101000000 000LLLLLLL LL
 25.0000   0111000000 000LLLLLLL LH
 26.0000   1111000000 000LLLLLLL LH
 27.0000   1111111111 111LLLLLLL LH

 28.0000   1111000000 000LLLLLLL LL
 29.0000   0111000000 000LLLLLLL LH
```

DATE 06-FEB-78 TIME 20:48 PATTERN FILE PA212.PAT;WCT

```
1                    0          0
  TO                 1          2
      22  1234567890 1234567890 12

30.0000   0111011111 111LLLLLLL LH
31.0000   0101011111 111HHHHHHH HL
32.0000   1101011111 111HHHHHHH HL
33.0000   1101111111 111HHHHHHH HL
34.0000   1100111111 111HHHHHHH HH

35.0000   1100011111 111HHHHHHH HL
36.0000   1100111111 111HHHHHHH HL
37.0000   0100111111 111LLLLLLL LH
38.0000   1100111111 111LLLLLLL LH
39.0000   1100011111 111LLLLLLL LL

40.0000   1100111111 111LLLLLLL LL
41.0000   1100011111 111LLLLLLL LL
42.0000   1101011111 111HHHHHHH HL
43.0000   1100011111 111HHHHHHH HH
44.0000   1101011111 111HHHHHHH HL

45.0000   1101000000 000LLLLLLL LL
46.0000   0101000000 000LLLLLLL LL
47.0000   1101000000 000LLLLLLL LL
48.0000   1001000000 000LLLLLLL LL
49.0000   0001000000 000LLLLLLL LL

50.0000   1001011111 111LLLLLLL LL
51.0000   0001011111 111LLLLLLL LL
52.0000   0001000000 000LLLLLLL LL
53.0000   1101011111 111HHHHHHH HL
54.0000   1001011111 111HHHHHHH HL

55.0000   1001000000 000HHHHHHH HL
56.0000   1001011111 111HHHHHHH HL
57.0000   1101010000 000HLLLLLL LL
58.0000   1101001000 000LHLLLLL LL
59.0000   1101000100 000LLHLLLL LL

60.0000   1101000010 000LLLHLLL LL
61.0000   1101000001 000LLLLHLL LL
62.0000   1101000000 100LLLLLHL LL
63.0000   1101000000 010LLLLLLH LL
64.0000   1101000000 001LLLLLLL HL

65.0000   1101100000 000LLLLLLL LL
66.0000   1100100000 000LLLLLLL LH
67.0000   1000100000 0001111111 1H
68.0000   1000111111 1111111111 1H
69.0000   1100111111 111HHHHHHH HH

70.0000   0000111111 1111111111 1H
71.0000   0000011111 1111111111 1H
```

```
DATE  06-FEB-78      TIME  20:48      PATTERN FILE   P8212.PAT;WCT

 1                     0           0
   TO                  1           2
       22  1234567890 1234567890 12

 72.0000   1000011111 1111111111 1H
 73.0000   0000011111 1111111111 1H
 73.0001   *
 73.0002   *     THE FIRST FOUR VECTORS ARE REPEATED SO ALL ERRORS
 73.0003   *     WITH NO ERRORS DETECTED ON GOOD DEVICES.

 73.0004   *
 74.0000   0100000000 000LLLLLLL LH
 75.0000   0101000000 000LLLLLLL LL
 76.0000   0001000000 000LLLLLLL LL
 77.0000   1001000000 000LLLLLLL LL

 77.0001   *  THE FOLLOWING VECTORS ARE FOR TIMING TESTS
 77.0002   *
 77.0003   * VECTORS FOR TPHL1 AND TPLH1
 77.0004   *
 78.0000   1101010000 0000000000 00

 79.0000   1101001000 0000000000 00
 80.0000   1101000100 0000000000 00
 81.0000   1101000010 0000000000 00
 82.0000   1101000001 0000000000 00
 83.0000   1101000000 1000000000 00

 84.0000   1101000000 0100000000 00
 85.0000   1101000000 0010000000 00
 85.0001   *
 85.0002   * VECTORS FOR TPHL2 AND TPLH2
 85.0003   *

 86.0000   1001100000 0000000000 00
 87.0000   1001110000 0000000000 00
 88.0000   1001101000 0000000000 00
 89.0000   1001100100 0000000000 00
 90.0000   1001100010 0000000000 00

 91.0000   1001100001 0000000000 00
 92.0000   1001100000 1000000000 00
 93.0000   1001100000 0100000000 00
 94.0000   1001100000 0010000000 00
 95.0000   1001100000 0000000000 00

 95.0001   *
 95.0002   * VECTORS FOR TPHL3 AND TPHL3
 95.0003   *
 96.0000   1001100000 0000000000 00
 97.0000   1011100000 0000000000 00

 97.0001   *
 97.0002   * VECTORS FOR TPHL4 AND TPLH4
```

```
DATE  06-FEB-78      TIME  20:48      PATTERN FILE   P8212.PAT;WCT

  1                    0           0
    TO                 1           2
        22  1234567890 1234567890 12

 97.0003  *
 98.0000   1111000000 0000000000 00
 99.0000   1111010000 0000000000 00
100.0000   1111001000 0000000000 00
101.0000   1111000100 0000000000 00

102.0000   1111000010 0000000000 00
103.0000   1111000001 0000000000 00
104.0000   1111000000 1000000000 00
105.0000   1111000000 0100000000 00
106.0000   1111000000 0010000000 00

107.0000   1111000000 0000000000 00
107.0001  *
108.0000   1101000000 0000000000 00
109.0000   1101010000 0000000000 00
110.0000   1101001000 0000000000 00

111.0000   1101000100 0000000000 00
112.0000   1101000010 0000000000 00
113.0000   1101000001 0000000000 00
114.0000   1101000000 1000000000 00
115.0000   1101000000 0100000000 00

116.0000   1101000000 0010000000 00
117.0000   1101000000 0000000000 00
117.0001  *
117.0002  *  VECTORS FOR TPHL5
117.0003  *

118.0000   1101110000 0000000000 00
119.0000   1101101000 0000000000 00
120.0000   1101100100 0000000000 00
121.0000   1101100010 0000000000 00
122.0000   1101100001 0000000000 00

123.0000   1101100000 1000000000 00
124.0000   1101100000 0100000000 00
125.0000   1101100000 0010000000 00
125.0001  *
125.0002  *   VECTORS FOR TPZL1 AND TPZL1

125.0003  *
126.0000   1010100000 0000000000 00
127.0000   1001100000 0000000000 00
127.0001  *
127.0002  *   VECTORS FOR TPZH1 AND TPHZ1

127.0003  *
128.0000   1010111111 1110000000 00
```

```
DATE  06-FEB-78      TIME  20:48      PATTERN FILE   PA212.PAT;WCT

  1                    0           0
    TO                 1           2
        22  1234567890 1234567890 12

 129.0000   1001111111 1110000000 00
```

DK0:A212.PIN:WCT DATE: 06-FEB-78 TIME: 20:50:49

LINE NUMBER	SECTOR NUMBER	PIN NAME	DUT PIN OR COMMENT
1.0000	1WAIO	SP1	
2.0000	5WAIO	SP2	
3.0000	9WAIO	SP3	
4.0000	13WAIO	SP4	
5.0000	17WAIO	SP5	
6.0000	21WAIO	SP6	
7.0000	25WAIO	SP7	
8.0000	29WAIO	SP8	
9.0000	33WAIO	SP9	
10.0000	37WAIO	SP10	
11.0000	41WAIO	SP11	
12.0000	45WAIO	SP12	
13.0000	49WAIO	SP13	
14.0000	53WAIO	SP14	
15.0000	57WAIO	SP15	
16.0000	61WAIO	SP16	
17.0000	2XAIO	SP17	
18.0000	6XAIO	SP18	
19.0000	10XAIO	SP19	
20.0000	14XAIO	SP20	
21.0000	18XAIO	SP21	
22.0000	22XAIO	SP22	
23.0000	26XAIO	SP23	
24.0000	30XAIO	SP24	

SOCKET CARD S/N 2010 WIRING LIST

DUT PIN	To	I/O PIN
1		1
2		5
3		9
4		13
5		17
6		21
7		25
8		29
9		33
10		37
11		41
12		45
13		49
14		53
15		57
16		61
17		2
18		6
19		10
20		14
21		18
22		22
23		26
24		30

SOCKET CARD I/O JUMPERS	
1 W I	1 W O
2 X I	2 X O
5 W I	5 W O
6 X I	6 X O
9 W I	9 W O
10 X I	10 X O
13 W I	13 W O
14 X I	14 X O
17 W I	17 W O
18 X I	18 X O
21 W I	21 W O
22 X I	22 X O
25 W I	25 W O
26 X I	26 X O
29 W I	29 W O
30 X I	30 X O
33 W I	33 W O
37 W I	37 W O
40 Z I	40 Z O
41 W I	41 W O
45 W I	45 W O
49 W I	49 W O
52 Z I	52 Z O
53 W I	53 W O
57 W I	57 W O
61 W I	61 W O

UNDER SOCKET CONNECTOR WIRING

C A 7	TO	D U T 24	C B 25	TO	C A 13
C A 8		D U T 24	C A 13		C A 14
C A 9		RING gnd	C A 11		C A 12
C A 10		RING gnd	* D U T 6		RING gnd
C B 25		RING gnd	* D U T 18		RING gnd

*2915 and 2916 devices only

APPENDIX C

TEST PROGRAM AND DATA FOR THE

TEKTRONIX 3260

FOR THE 2918

```
P2918.EDT;WCT                                   DISK NAME:  ETEC-12
DATE  07-FEB-78      TIME  10:49                PAGE   1 OF   3

   1.0000 * THIS TEST IS FOR THE 2918 DEVICE
   1.0100 * WRITTEN BY W.C.TAYLOR
   1.1000 * PAP TABLE USED WITH THIS PROGRAM IS P2918.PIN;WCT
   1.2000 * TEST PATTERN FILE USED WITH THIS PROGRAM IS P2918.PAT;WCT
   1.2100 * SOCKET CARD IS S/N 2012
   1.3000 *
   1.4000 * PART 2 CONTAINS PINLISTS AND ARRAYS
   1.5000 * PART 3 CONTAINS FUNCTIONAL TESTS AND HIGH IMPEDANCE OUTPUT TESTS
   1.6000 * PART 50 CONTAINS PASS/FAIL SORT ROUTINE, OUTPUT ROUTINE

   2.0000   PINLIST INS=SP1,SP4,SP12,SP15,SP7,SP9
   2.0100   PINLIST QOUTS=SP2,SP5,SP11,SP14
   2.0110   PINLIST DOG=SP3,SP6
   2.0120   PINLIST CAT=SP10,SP13
   2.0200   PINLIST YOUTS=SP3,SP6,SP10,SP13
   2.0300   PINLIST OUTS=QOUTS,YOUTS
   2.2000   PINLIST ALL=INS,SP2,SP3,SP5,SP6,SP11,SP10,SP14,SP13
   2.3000   PINLIST GND=SP8
   2.4000   PINLIST VCC=SP16
   2.4100
   2.4200   ARRAY IIH(2),IIH1(2),IIH2(2),IIH3(2)
   2.4210   IARRAY OUTSOL(11)
   2.4300
   2.4410   OUTSOL(1)=3
   2.4420   OUTSOL(2)=10
   2.4430   OUTSOL(3)=3
   2.4440   OUTSOL(4)=10
   2.4450   OUTSOL(5)=6
   2.4460   OUTSOL(7)=13
   2.4470   OUTSOL(9)=6
   2.4480   OUTSOL(11)=13
   2.5000
   2.6000   SUBROUTINE EVS6(0),DVS6(0) :MC3
   2.7000   FUNCTION MVS6(V), IVS6(0) :MC3
   2.8000   SUBROUTINE CRDATE(V),CRTIME(V):TIME
   2.9000   FUNCTION GETBIT(I,V,V,V):BARRAY
```

```
2.9010    SUBROUTINE BARRAY(I,V,V,V):BARRAY
2.9020    SUBROUTINE SREAD(P,V,V,V,V,I,V):SREAD
2.9030    IARRAY BER(70),PIN(9),C(40),D(40)
2.9031    ARRAY FF(40,9),V(40)
2.9040    BARRAY(BFR,2,8,36)
2.9050
2.9060
2.9070 *          LABEL DATE AND TIME DATA IS TAKEN
2.9080
2.9090
2.9091    PRINT <4> ERASE
2.9100    PRINT <4> CR,"DATE: "
2.9110    CRDATE(4)
2.9120    PRINT <4> CR,"TIME: "
2.9130    CRTIME(4)
2.9140    PRINT <4> CR,"THIS TEST IS FOR THE 2918 DEVICE",CR

3.0000    INITIALIZE
3.0100    VS6=5V AT 120MA
3.0200    FVS6
3.0300    X=MVS6(10)
3.0400    Y=IVS6
3.0500    IF(10MA<Y<120MA) 3.10,3.10,3.06
3.0600    PRINT"DEVICE DRAWS MORE THAN 120MA OF CURRENT",CR
3.0700    PRINT CR,CR,"CHECK TO ENSURE DEVICE IS INSTALLED CORRECTLY",CR
3.0800    DVS6
3.0900    STOP
3.1000    IF(4.75V<X<5.25V) 3.11,3.17,3.14
3.1100    PRINT"SUPPLY VOLTAGE IS <4.75V",CR
3.1200    DVS6
3.1300    STOP
3.1400    PRINT"SUPPLY VOLTAGE IS >5.25V",CR
3.1500    DVS6
3.1600    STOP
3.1700    CONTINUE
3.1800    CYCLE=500NS
3.1900    HICOMPARE=200NS FOR 100NS
3.2000    LOCOMPARE=200NS FOR 100NS
3.2100    CONNECT INPUT TO DRIVER ON INS
```

```
3.2200   CONNECT OUTPUT TO COMPARATOR ON OUTS
3.2300   HICOMPARE=2.5V ON OOUTS
3.2400   HICOMPARE=2.4V ON YOUTS
3.2500   LOCOMPARE=0.5V ON OUTS
3.2600   HIDRIVE=2.0V ON INS
3.2700   LODRIVE=0.8V ON INS
3.2800   LOAD DISK P2918 TO ALL WITH FI,CM
3.2900   FORCE INS WITH PATTERN
3.3000   COMPARE OUTS WITH PATTERN
3.3010   MASK OUTS WITH PATTERN
3.3100   MOVE REGISTER (1,35) TO ALL WITH FI,CM AND SAVE ERRORS
3.3200   X=ERROR
3.3400   IF (NOT X) 3.37
3.3600   GOTO 50.00
3.3700   PRINT CR,CR,"PASSED FUNCTIONAL TESTS",CR
3.3701   LOAD DISK P2918 TO ALL WITH FI,CM
3.3702   DISCONNECT OUTPUT FROM COMPARATOR ON OUTS
3.3710   FORCE INS WITH PATTERN
3.3720   MOVE REGISTER (1,29) TO ALL WITH FI,CM
3.3730   LOOP  3.385 J=1,2
3.3750   SETUP TO MEASURE CURRENT ON DOG (J) FROM VS3=0.4V AT 100UA
3.3760   IIH(J)=CURRENT
3.3770   UNSET TO MEASURE CURRENT ON DOG (J) FROM VS3
3.3800   SETUP TO MEASURE CURRENT ON CAT (J) FROM VS3=2.4V AT 100UA
3.3810   WAIT 1S
3.3820   IIH1(J)=CURRENT
3.3830   UNSET TO MEASURE CURRENT ON CAT (J) FROM VS3
3.3850   CONTINUE
3.3860   FORCE INS WITH PATTERN
3.3870   MOVE REGISTER (1,31) TO ALL WITH FI,CM
3.3880   LOOP 3.400 J=1,2
3.3900   SETUP TO MEASURE CURRENT ON DOG (J) FROM VS3=2.4V AT 100UA
3.3910   IIH2(J)=CURRENT
3.3920   UNSET TO MEASURE CURRENT ON DOG (J) FROM VS3
3.3950   SETUP TO MEASURE CURRENT ON CAT (J) FROM VS3=.4V AT 100UA
3.3960   WAIT 1S
3.3970   IIH3(J)=CURRENT
3.3980   UNSET TO MEASURE CURRENT ON CAT (J) FROM VS3
3.4000   CONTINUE
```

```
3.4010    LOOP 3.414 J=1,2
3.4020    IF(-50UA<IIH(J)<50UA) 3.404
3.4030    PRINT "FAILED OUTPUT CURRENT ON PIN= ",OUTSOL(J*(J+1)-1),IIH(J):F3,"A",CR
3.4031    GOTO 3.8
3.4040    PRINT CR,CR, "PASSED OUTPUT CURRENT ON PIN= ",OUTSOL(J*(J+1)-1),IIH(J):F3,"A",CR
3.4050    IF(-50UA<IIH1(J)<50UA) 3.407
3.4060    PRINT "FAILED OUTPUT CURRENT ON PIN= ",OUTSOL(J*(J+2)-1),IIH1(J):F3,"A",CR
3.4061    GOTO 3.8
3.4070    PRINT "PASSED OUTPUT CURRENT ON PIN= ",OUTSOL(J*(J+2)-1),IIH1(J):F3,"A",CR
3.4080    IF(-50UA<IIH2(J)<50UA) 3.410
3.4090    PRINT "FAILED OUTPUT CURRENT ON PIN= ",OUTSOL(J*(J+3)-1),IIH2(J):F3,"A",CR
3.4091    GOTO 3.8
3.4100    PRINT "PASSED OUTPUT CURRENT ON PIN= ",OUTSOL(J*(J+3)-1),IIH2(J):F3,"A",CR
3.4110    IF(-50UA<IIH3(J)<50UA) 3.413
3.4120    PRINT "FAILED OUTPUT CURRENT ON PIN= ",OUTSOL(J*(J+4)-1),IIH3(J):F3,"A",CR
3.4121    GOTO 3.8
3.4130    PRINT "PASSED OUTPUT CURRENT ON PIN= ",OUTSOL(J*(J+4)-1),IIH3(J):F3,"A",CR
3.4140    CONTINUE
3.8000    DISCONNECT INPUT FROM DRIVER ON INS
3.8100    DISCONNECT OUTPUT FROM COMPARATOR ON OUTS
3.8200    DVS6
3.8300    STOP
```

```
50.0000 *              SORT FAILING FUNCTIONAL TESTS
50.0100 *
50.0200    SREAD (OUTS,0,0,5,31,BER,2)
50.0300    PRESET PIN(1)=2,5,11,14,3,6,10,13
50.0400    A=1
50.0500    LOOP 50.15 J=1,31
50.0600    S=0
50.0650    LOOP 50.1 I=1,8
50.0700    IF (NOT GETBIT(BER,1,I,J)) 50.1
50.0800    S=S+1
50.0900    FF(A,S)=I
50.1000    CONTINUE
50.1100    IF (S EQ 0) 50.15
50.1200    C(A)=J
50.1300    D(A)=S
50.1400    A=A+1
50.1500    CONTINUE
50.1600    A=A-1
50.1700
50.1800    PRINT <5> CR,CR, "FAILED ",A:I," OUT OF 31 FUNCTIONAL TESTS",CR
50.1900    PRINT <5> "THE FOLLOWING FUNCTIONAL TESTS FAILED ",CR
50.2000    PRINT <5> "VECTOR NUMBER :  FAILING PINS",CR
50.2100    LOOP 50.25 J=1,A
50.2200    PRINT <5> CR,C(J):I,": "
50.2300    LOOP 50.24 I=1,D(J)
50.2400    PRINT <5> PIN(FF(J,I)):I
50.2500    CONTINUE
50.3000    GOTO 3.3701
```

```
DATE  06-FEB-78      TIME  20:47      PATTERN FILE   P291A.PAT;WCT

  1                    0
    TO                 1
        14  1234567890 1234

  0.0001  *
  0.0002  *
  0.0003  *
  0.0004  *  11        1111
  0.0005  *142579 23561043

  0.0006  *
  0.0007  *THE FOLLOWING ARE THE DEVICE PIN NAMES
  0.0008  *
  0.0009  *
  0.0010  *

  0.0011  *    -
  0.0012  *DDDDOC QYQYQYQY
  0.0013  *0123EP 00112233
  0.0014  *
  0.0015  *

  1.0000    0101011111 1111
  2.0000    0101001111 1111
  3.0000    010101LLHH LLHH
  4.0000    010100LLHH LLHH
  5.0000    010101LLHH LLHH

  6.0000    101001LLHH LLHH
  7.0000    101000LLHH LLHH
  8.0000    101001HHLL HHLL
  9.0000    101000HHLL HHLL
 10.0000    101001HHLL HHLL

 11.0000    010101HHLL HHLL
 12.0000    101001HHLL HHLL
 13.0000    010101HHLL HHLL
 14.0000    010100HHLL HHLL
 15.0000    101000HHLL HHLL

 16.0000    010100HHLL HHLL
 17.0000    010101LLHH LLHH
 18.0000    101001LLHH LLHH
 19.0000    010101LLHH LLHH
 20.0000    010100LLHH LLHH
```

1 TO 14	0 1 1234567890 1234
21.0000	111100LLHH LLHH
22.0000	000000LLHH LLHH
23.0000	000001LLLL LLLL
24.0000	110001LLLL LLLL
25.0000	110000LLLL LLLL
26.0000	110001HHHH LLLL
27.0000	001101HHHH LLLL
28.0000	001100HHHH LLLL
29.0000	001110H1H1 L1L1
30.0000	001101LLLL HHHH
31.0000	001111L1L1 H1H1
32.0000	0000000000 0000
33.0000	0000000000 0000
34.0000	0000000000 0000
35.0000	0000000000 0000

DK0:P2918.PIN:WCT DATE: 06-FEB-78 TIME: 20:50:31

LINE NUMBER	SECTOR NUMBER	PIN NAME	OUT PIN OR COMMENT
1.0000	1WAIO	SP1	D0
2.0000	5WAIO	SP2	Q0
3.0000	9WAIO	SP3	Y0
4.0000	13WAIO	SP4	D1
5.0000	17WAIO	SP5	Q1
6.0000	21WAIO	SP6	Y1
7.0000	25WAIO	SP7	OEBAR
8.0000	29WAIO	SP8	GND
9.0000	33WAIO	SP9	CLOCK CP
10.0000	37WAIO	SP10	Y2
11.0000	41WAIO	SP11	Q2
12.0000	45WAIO	SP12	D2
13.0000	49WAIO	SP13	Y3
14.0000	53WAIO	SP14	Q3
15.0000	57WAIO	SP15	D3
16.0000	61WAIO	SP16	VCC
17.0000	* THIS IS A PAP FOR 2918		

SOCKET CARD S/N 2012 WIRING LIST

DUT PIN to I/O PIN

1	1
2	5
3	9
4	13
5	17
6	21
7	25
8	29
9	33
10	37
11	41
12	45
13	49
14	53
15	57
16	61

SOCKET CARD I/O JUMPERS

1 WI	to	1 WO
5 WI		5 WO
9 WI		9 WO
13 WI		13 WO
17 WI		17 WO
21 WI		21 WO
25 WI		25 WO
29 WI		29 WO
33 WI		33 WO
37 WI		37 WO
41 WI		41 WO
45 WI		45 WO
49 WI		49 WO
53 WI		53 WO
54 WI		54 WO
57 WI		57 WO
58 WI		58 WO
61 WI		61 WO

UNDERSOCKET CONNECTOR TO DUT PIN AND GROUND

CA 7	DUT 16
CA 8	DUT 16
CA 9	Ring Gnd
CA 10	Ring Gnd
CB 25	Ring Gnd
DUT 8	Nearest Ring Gnd

APPENDIX D

TEST PROGRAMS AND DATA

FOR THE TEKTRONIX 3260

FOR THE 2915, 2916 AND 2917

i. Tektronix 3260 test for the 2915

The following pages contain the test program, pattern file, and pin assignment program for the 2915.

```
DK0:P2915.EDT;WCT    DATE: 22-FEB-78    TIME: 13:51:03    PAGE  1

1.0100 *  2915 QUAD 3-STATE TRANSCEIVER WITH INTERFACE LOGIC
1.0200 *
1.0300 *                    WRITTEN BY D.A. O'CONNOR      26/OCT/77
1.0400 *
1.0500 *
1.0600 *  TEST PATTERN FILE NAME FOR THIS DEVICE IS P2915A.PAT;WCT
1.0700 *
1.0800 * PIN ASSIGNMENT FILE NAME FOR THIS DEVICE IS P2915.PIN;WCT
1.0900 *
1.1000 *  TEST STATION SOCKET CARD # IS ETEC S\N 2010
1.1100 *
1.1200 *
1.1300
1.1400 *        TABLE OF CONTENTS
1.1500 *
1.1600 *  PART     DESCRIPTION OF CONTENTS
1.1700
1.1800 *    1      DEVICE DISCRIPTION
1.1900 *    2      PINLISTS, ARRAYS, AND CONSTANTS
1.2000 *    3      FUNCTIONAL TESTS
1.2100 *   4/5     OUTPUT HIGH IMPEDANCE TESTS
1.2200 *    6      OUTPUT LEAKAGE TEST RESULTS
1.2400 *   50      PASS/FAIL FUNCTIONAL TEST SORT ROUTINE

2.0100 *  PINLIST INDICATES TEST PIN #
2.0200 *
2.0300 *
2.0400    PINLIST EN =P1,P12,P11
2.0500    PINLIST AIN = P4,P8,P16,P20
2.0600    PINLIST BIN = P3,P9,P15,P21
2.0700    PINLIST BUS = P5,P7,P17,P19
2.0800    PINLIST REC = P2,P10,P14,P22
2.0900    PINLIST INS1 = P13,AIN,BIN,P23,EN
2.0910    PINLIST INS2 = P13,AIN,BIN,P23,EN,BUS
2.1000    PINLIST OUTS1 = BUS,REC
2.1010    PINLIST OUTS2 = REC
2.1100    PINLIST ALL = INS1,OUTS1
```

```
2.1300    SUBROUTINE EVS6(0),DVS6(0):MC3
2.1400    FUNCTION MVS6(V),IVS6(0):MC3
2.1500    SUBROUTINE CRDATE(V),CRTIME(V):TIME
2.1600    SUBROUTINE BARRAY(I,V,V,V):BARRAY
2.1700    SUBROUTINE SREAD(P,V,V,V,V,I,V):SREAD
2.1800    FUNCTION GETBIT(I,V,V,V):BARRAY
2.1900    FUNCTION CHARI(V):STRING
2.2000    IARRAY BER(86),PIN(10),C(70),D(70)
2.2100    ARRAY FF(70,10)
2.2200    BARRAY(BER,2,8,59)
2.2300    ARRAY VALUE(20,20),V(60)
2.2400    PRESET PIN(1)=5,7,17,19,2,10,14,22
2.2500
2.2600    LOOP 2.3 I=1,20
2.2700    LOOP 2.29 J=1,20
2.2800    VALUE(I,J)=0.0
2.2900    CONTINUE
2.3000    CONTINUE
2.3100 *
2.3200 *
2.3300    PRINT <5> ERASE
2.3400    PRINT <5> CR,"DATE: "
2.3410    CRDATE(5)
2.3420    PRINT <5> CR,"TIME: "
2.3430    CRTIME(5)
2.3440    PRINT <5> CR
2.3450    PRINT <5> CR,CR,"THIS TEST IS FOR THE 2915 DEVICE",CR,CR
2.3500 *
2.3600 *
2.3700 *
2.3800 *     SET NUMBER OF TEST VECTORS TO BE USED
2.3900 *
2.4000    VECT = 59

3.0100 *    *** POWERSUPPLY CHECK ***
3.0200 *
3.0300 *
3.0400    INITIALIZE
3.0500 *
```

```
3.0800    VS6 = 5V AT 95MA
3.0900    EVS6
3.1000    X = MVS6(10)
3.1100    Y = IVS6
3.1200    IF(5MA<Y<95MA) 3.19,3.19,3.15
3.1300    PRINT <4> "DEVICE DRAWS LESS THAN 5MA OF CURRENT"
3.1400    GOTO 3.16
3.1500    PRINT <4> "DEVICE DRAWS MORE THAN 95MA OF CURRENT"
3.1600    PRINT <4> CR,CR,"CHECK TO ENSURE DEVICE IS INSTALLED CORRECTLY",CR
3.1700    GOTO 7.43
3.1800
3.1900    IF(4.75V<X<5.25V)3.2,3.26,3.23
3.2000    PRINT <4> "SUPPLY VOLTAGE IS <4.75V",CR
3.2100    GOTO 7.43
3.2200
3.2300    PRINT <4> "SUPPLY VOLTAGE IS > 5.25V",CR
3.2400    GOTO 7.43
3.2500
3.2600    CONTINUE
3.2700 *
3.2800 *    *** I / O SETUP ***
3.2900 *
3.3000    CYCLE = 500NS
3.3100    HICOMPARE = 200NS FOR 100NS
3.3200    LOCOMPARE = 200NS FOR 100NS
3.3300    CONNECT INPUT TO DRIVER ON INS1
3.3400    CONNECT OUTPUT TO COMPARATOR ON OUTS1
3.3500    HICOMPARE = 2.4V ON OUTS1
3.3600    LOCOMPARE = 0.4V ON OUTS1
3.3700    HIDRIVE = 2.0V ON INS1
3.3800    LODRIVE = 0.8V ON INS1
3.3900 *
3.4000 *    **** 2915 TEST PATTERN FILE ***
3.4100 *
3.4200    LOAD DISK P2915A TO ALL WITH FI,CM
3.4300 *
3.4400 *
3.4500    FORCE INS1 WITH PATTERN
```

```
3.4600    COMPARE OUTS1 WITH PATTERN
3.4700    MASK OUTS1 WITH PATTERN
3.4800
3.4900 *
3.5000    MOVE REGISTER (VECT) TO ALL WITH FI,CM AND SAVE ERRORS
3.5010    H = 55
3.5020    K = 0
3.5030    A = 1
3.5100 *
3.5200    X=ERROR
3.5300    IF (NOT X)3.74
3.5400 *
3.5500    PRINT <4> "FAILED FUNCTIONAL TEST ",CR
3.5600    GOTO 50.03
3.5700    PRINT <4> "DO YOU WANT TO CONTINUE?",CR
3.5800    ANS=CHAR1(1)
3.5900    IF (ANS EQ 89) 3.63
3.6000    IF (ANS EQ 78) 3.66
3.6100    PRINT <4> " PLEASE ANSWER YES OR NO.",CR
3.6200    GO TO 3.58
3.6300    GOTO 4.01
3.6301    CONTINUE
3.6320    DISCONNECT OUTPUT FROM COMPARATOR ON BUS
3.6321    FORCE P11 WITH ONE
3.6330    CONNECT INPUT TO DRIVER ON BUS
3.6370    HIDRIVE = 2.0V ON BUS
3.6380    LODRIVE = 0.8V ON BUS
3.6390    LOAD DISK P2915A (60,67) TO ALL WITH FI,CM
3.6400    FORCE INS2 WITH PATTERN
3.6410    COMPARE OUTS2 WITH PATTERN
3.6420    MASK OUTS2 WITH PATTERN
3.6425    MASK BUS WITH ONE
3.6430    MOVE REGISTER (8) TO ALL WITH FI,CM AND SAVE ERRORS
3.6431    H = 4
3.6432    K = 59
3.6440    G=ERROR
3.6441    F = F+G
3.6450    IF (NOT G)3.8
3.6451    GOTO 50.01
```

```
3.6500 *
3.6600    PRINT <4> " END OF THE 2915 TEST ",CR
3.6700    PRINT <4> CR,CR
3.6800    PRINT <4> "*************************************************",CR
3.6900    PRINT <4> "*  FAILED FUNCTIONAL TESTS                      *",CR
3.7000    PRINT <4> "*  ",A:I," OUT OF ",63:I," TESTS                *",CR
3.7100    PRINT <4> "*                                               *",CR
3.7200    PRINT <4> "*************************************************",CR
3.7300    STOP
3.7400    PRINT <4> "PASSED FUNCTIONAL TEST PART 1 ",CR
3.7500    CONTINUE
3.8000    PRINT <4> "PASSED FUNCTIONAL TEST PART 2",CR
3.9000    IF (F)50,17

4.0100    DISCONNECT OUTPUT FROM COMPARATOR ON OUTS1
4.0110    DISCONNECT INPUT FROM DRIVER ON INS2
4.0200    VS6=5.5V AT 95MA
4.0300    K=MVS6(10)
4.0400    IF(5.445<K<5.555) 4.11
4.0500    PRINT <4> CR," *** FAILED POWER SUPPLY VERIFICATION TEST **"
4.0600
4.0700 *
4.0800 *    HIGH IMPEDANCE TEST ON OUTPUTS
4.0900 *
4.1000 *
4.1100    HIDRIVE = 2.0V ON INS1
4.1200    LODRIVE = 0.8V ON INS1
4.1300 *
4.1400 *    **** 2915 TEST PATTERN FILE ***
4.1500 *
4.1600    LOAD DISK P2915A TO ALL WITH FI,CM
4.1700 *
4.1800 *
4.1900    FORCE INS1 WITH PATTERN
4.2000 *
4.2100    Z=10
4.2200    P=1
4.2300    CALL 5.25
4.2400    Z=11
```

```
4.2500      P=2
4.2700      CALL 5.25
4.2750      P=11
4.2800      CALL 5.42
4.2810      Z=20
4.2820      P=12
4.2850      CALL 5.42
4.2900      Z=23
4.3000      P=3
4.3100      CALL 5.25
4.3200      Z=24
4.3300      P=4
4.3500      CALL 5.25
4.3550      P=13
4.3600      CALL 5.42
4.3700      Z=51
4.3800      P=5
4.4000      CALL 5.25
4.4050      P=14
4.4100      CALL 5.42
4.4200      Z=52
4.4300      P=6
4.4500      CALL 5.25
4.4550      P=15
4.4600      CALL 5.42
4.4700      Z=54
4.4800      P=7
4.5000      CALL 5.25
4.5050      P=16
4.5100      CALL 5.42
4.5200      Z=55
4.5300      P=8
4.5500      CALL 5.25
4.5550      P=17
4.5600      CALL 5.42
4.5700      GOTO 6.06
```

```
5.0100 *    ****  OUTPUT LEAKAGE TEST  ****
5.0200 *
5.0300 *
5.0400 *
5.0500 *  Z VALUE INDICATES VECTOR # OF PATTERN
5.0600 *
5.0700 *  ARRAY VALUE((A,B) WILL CONTAIN OUTPUT LEAKAGE DATA
5.0800 *
5.0900 *    FOR BUS OUTPUTS  A  = VECTOR #
5.1000 *
5.1100 *     BUS0>BUS3 LEAKAGE AT VOLTAGE
5.1200 *        B = 1>4 AT 0.4V
5.1300 *        B = 5>8 AT 2.4V
5.1400 *        B = 9>12 AT 4.5V
5.1500 *
5.1600 *    FOR REC OUTPUTS  A = VECTOR # BEGINS AT 11
5.1700 *
5.1800 *    R0>R3   LEAKAGE AT VOLTAGE
5.1900 *        B = 1>4 AT 0.4V
5.2100 *
5.2200 *
5.2300 *  THE FOLLOWING PERFORMS OUTPUT LEAKAGE TESTS ON BUS OUTPUTS
5.2400 *
5.2500    V(P)=Z
5.2600    MOVE REGISTER (Z) TO ALL WITH FI,CM
5.2700    LOOP 5.39 I = 1,4
5.2800 *
5.2900    SETUP TO MEASURE CURRENT ON BUS(I) FROM VS4=4.5V AT 300UA
5.3000    VALUE(P,I+8)=CURRENT
5.3200 *
5.3300    VS4=2.4V AT 100UA
5.3400    VALUE(P,I+4)=CURRENT
5.3600 *
5.3700    VS4=0.4V AT -300UA
5.3800    VALUE(P,I)=CURRENT
5.3900    UNSET TO MEASURE CURRENT ON BUS(I) FROM VS4
5.4000 *
5.4100    RETURN
5.4200
```

```
5.4300 *  THE FOLLOWING PERFORMS OUTPUT LEAKAGE TESTS ON REC OUTPUTS
5.4400
5.4500    V(P)=Z
5.4600    LOOP 5.54 I = 1,4
5.4700 *
5.4800    SETUP TO MEASURE CURRENT ON REC(I) FROM VS4=2.4V AT 40UA
5.4900    VALUE(P,I+4)=CURRENT
5.5000    VS4=0.4V AT 20UA
5.5100 *
5.5300    VALUE(P,I)=CURRENT
5.5400    UNSET TO MEASURE CURRENT ON REC(I) FROM VS4
5.5500 *
5.5600    RETURN

6.0100 *   **** OUTPUT LEAKAGE RESULTS ****
6.0200 *
6.0300 *
6.0400 *
6.0600    PRINT <5> CR,CR,CR,CR,CR,CR,CR,CR,CR," OUTPUT LEAKAGE CURRENT TEST RESULTS",CR,CR
6.0700    PRINT <5> "BUS OUTPUT RESULTS",CR,CR
6.0800    PRINT <5> "  OUTPUT LIMITS ARE   200UA       50UA          100UA          ",CR
6.0900    PRINT <5> "VECTOR # OUTPUT #    V0=0.4V   V0=2.4V        V0=4.5V",CR
6.1000    PRINT <5> "-------- ----------  --------  --------      --------",CR
6.1010    B=0
6.1100    LOOP 6.32 P=1,8
6.1200    PRINT <5> CR,"  ",V(P):I2
6.1300    LOOP 6.301 I=1,4
6.1400    PRINT <5> "     ",(I-1):I1,"     ",VALUE(P,I)
6.1500    IF (-200UA<VALUE(P,I)<200UA) 6.19
6.1600    PRINT <5> " FAILED"
6.1700    B=1
6.1800    GOTO 6.2
6.1900    PRINT <5> "       "
6.2000    PRINT <5> VALUE(P,I+4)
6.2100    IF (-50UA<VALUE(P,I+4.01)<50UA) 6.25
6.2200    PRINT <5> " FAILED"
6.2300    B=B+1
6.2400    GOTO 6.26
6.2500    PRINT <5> "       "
```

```
6.2600    PRINT <5> VALUE(P,I+8)
6.2700    IF (-100US<VALUE(P,I+8)<100UA) 6.301
6.2800    PRINT <5> " FAILED"
6.2900    R=1
6.3010    PRINT <5> CR,"        "
6.3200    CONTINUE
6.3300    R=0
6.3400    PRINT <5> CR,CR,CR,CR,CR,CR,CR,"RECEIVER OUTPUT RESULTS",CR,CR
6.3500    PRINT <5> "OUTPUT LIMITS ARE    20UA                  20UA ",CR
6.3600    PRINT <5> "VECTOR # OUTPUT #   V0=0.4V               V0=2.4V",CR
6.3700    PRINT <5> "-------- --------  -------               -------",CR
6.3800    LOOP 6.53 P=11,17
6.3900    PRINT <5> CR,V(P):I2
6.4000    LOOP 6.52 I=1,4
6.4100    PRINT <5> "     ",(I-1):I1,"     ",VALUE(P,I)
6.4200    IF (-20UA<VALUE(P,I)<20UA) 6.46
6.4300    PRINT <5> " FAILED"
6.4400    R=1
6.4500    GOTO 6.47
6.4600    PRINT <5> "        "
6.4700    PRINT <5> "     ",VALUE(P,I+4)
6.4800    IF (-20UA<VALUE(P,I+4)<20UA ) 6.52
6.4900    PRINT <5> " FAILED"
6.5000    R=1
6.5200    PRINT <5> CR,"      "
6.5300    CONTINUE
6.5600    RETURN

7.0100 *   **** TOTAL TEST RESULTS ****
7.0200 *
7.0300 *
7.0400    PRINT <5> CR,CR,CR," SUMMARY OF TEST RESULTS ",CR,CR
7.0500 *
7.0600    IF(0<R<1000) 7.07
7.0700    PRINT <5> "*************************************************",CR
7.0800    PRINT <5> "*                                               *",CR
```

```
7.0900   IF(X) 7.13
7.1000   PRINT <5> "*          PASSED FUNCTIONAL TESTS                *",CR
7.1100   PRINT <5> "*                                                 *",CR
7.1200   GOTO 7.16
7.1300   PRINT <5> "*          FAILED FUNCTIONAL TESTS                *",CR
7.1500   PRINT <5> "*                                                 *",CR
7.1600   IF(R) 7.2
7.1700   PRINT <5> "*     PASSED OUTPUT LEAKAGE ON BUS OUTPUTS        *",CR
7.1800   PRINT <5>       "*                                                    *",CR
7.1900   GOTO 7.23
7.2000   PRINT <5> "*      FAILED OUTPUT LEAKAGE ON BUS OUTPUTS       *",CR
7.2200   PRINT <5> "*                                                 *",CR
7.2300   IF(R) 7.27
7.2400   PRINT <5> "*    PASSED OUTPUT LEAKAGE ON RECEIVER OUTPUTS    *",CR
7.2500   PRINT <5> "*                                                 *",CR
7.2600   GOTO 7.3
7.2700   PRINT <5> "*    FAILED OUTPUT LEAKAGE ON RECEIVER OUTPUTS    *",CR
7.2900   PRINT <5> "*                                                 *",CR
7.3000   PRINT <5> "*                                                 *",CR
7.3100   PRINT <5> "*****************************************************",CR
7.3110   STOP

50.0100 *          SORT FAILING FUNCTIONAL TESTS
50.0200 *
50.0210   SREAD (OUTS2,0,0,5,H,BER,2)
50.0220   GOTO 50.05
50.0300   SREAD (OUTS1,0,0,5,H,BER,2)
50.0500   LOOP 50.16 J=1,H
50.0600   S=0
50.0700   LOOP 50.11 I=1,8
50.0800   IF (NOT GETBIT(BER,1,I,J)) 50.11
50.0900   S=S+1
50.1000   FF(A,S)=I
50.1100   CONTINUE
```

```
50.1200    IF (S EQ 0) 50.16
50.1300    C(A)=J+K
50.1400    D(A)=S
50.1500    A=A+1
50.1600    CONTINUE
50.1610    IF (K EQ 0) 3.6301
50.1620    GOTO 3.9
50.1700    A=A-1
50.1800
50.1900    PRINT <5> "THE FOLLOWING FUNCTIONAL TESTS FAILED ",CR
50.2000    PRINT <5> "VECTOR NUMBER :  FAILING PINS",CR
50.2100    LOOP 50.25 J=1,A
50.2200    PRINT <5> CR,C(J):I,":  "
50.2300    LOOP 50.24 I=1,D(J)
50.2400    PRINT <5> PIN(FF(J,I)):I2
50.2500    CONTINUE
50.2600    PRINT <5> CR,"FAILED ",A:I," OUT OF ",63:I,"  FUNCTIONAL TESTS",CR
50.2700    GOTO 3.57
```

```
DATE  22-FEB-78      TIME  13:18      PATTERN FILE  P2915A,PAT:WC1

 1                          0                 0
   TO                       1                 2
       24  1 2345 6789 0 1 2 3 4567 8901 23 4

  0.0001   * 2915 QUAD 3-STATE TRANSCEIVER
  0.0002   *      WITH INTERFACE LOGIC
  0.0003   *
  0.0004   *
  0.0005   * THE FOLLOWING ARE THE DEVICE PIN NAMES

  0.0006   *                          ----
  0.0007   *              D -         HHHH        GG
  0.0008   *              R R - -     UUUU        NN V
  0.0009   *  AAAA HHHH C L O H SSSS RRRR DD C
  0.0010   *S 0123 0123 P E E E 0123 0123 12 C

  0.0011   *
  0.0012   * THE FOLLOWING ARE THE DEVICE PIN NUMBERS
  0.0013   *
  0.0014   *1   12   12 2   1 1   11  112  1 2
  0.0015   *3 4860 3951 3 1 2 1 5779 2042 68 4

  1.0000    0 0000 1111 0 0 0 0 0000 0000 00 1
  2.0000    0 0000 1111 1 0 0 0 HHHH LLLL 00 1
  3.0000    0 0000 1111 0 0 0 0 HHHH LLLL 00 1
  4.0000    0 0000 1111 1 0 0 0 HHHH LLLL 00 1
  5.0000    0 1111 1111 1 0 0 0 HHHH LLLL 00 1

  6.0000    0 1111 1111 0 0 0 0 HHHH LLLL 00 1
  7.0000    0 0000 1111 0 0 0 0 HHHH LLLL 00 1
  8.0000    0 1111 1111 0 0 0 0 HHHH LLLL 00 1
  9.0000    0 1111 1111 0 1 0 0 HHHH LLLL 00 1
 10.0000    0 1111 1111 0 1 0 1 1111 LLLL 00 1

 11.0000    0 1111 1111 0 1 1 1 1111 1111 00 1
 12.0000    0 1111 1111 0 1 0 0 HHHH LLLL 00 1
 13.0000    0 1111 1111 1 1 0 0 LLLL LLLL 00 1
 14.0000    0 1111 1111 1 0 0 0 LLLL HHHH 00 1
 15.0000    1 1111 1111 1 0 0 0 LLLL HHHH 00 1

 16.0000    1 1111 1111 0 0 0 0 LLLL HHHH 00 1
 17.0000    1 1111 1111 1 0 0 0 LLLL HHHH 00 1
 18.0000    1 1111 0000 1 0 0 0 LLLL HHHH 00 1
 19.0000    1 1111 0000 0 0 0 0 LLLL HHHH 00 1
 20.0000    1 1111 1111 0 0 1 0 LLLL 1111 00 1

 21.0000    1 1111 0000 0 0 0 0 LLLL HHHH 00 1
 22.0000    1 1111 0000 0 1 0 0 LLLL HHHH 00 1
 23.0000    1 1111 0000 0 1 0 1 1111 HHHH 00 1
 24.0000    1 1111 0000 0 1 1 1 1111 1111 00 1
```

```
1                                   0                   0
  TO                                1                   2
      24   1 2345 6789 0 1 2 3 4567 8901 23 4

25.0000    1 1111 0000 0 1 0 0 LLLL HHHH 00 1

26.0000    1 1111 0000 1 1 0 0 HHHH HHHH 00 1
27.0000    0 0000 1111 0 1 0 0 HHHH HHHH 00 1
28.0000    0 0000 1111 1 1 0 0 HHHH HHHH 00 1
29.0000    0 0000 1111 0 0 0 0 HHHH LLLL 00 1
29.5000    1 0000 1111 0 0 0 0 HHHH LLLL 00 1
30.0000    1 0000 1111 0 1 0 0 HHHH LLLL 00 1
31.0000    1 0000 1111 1 1 0 0 LLLL LLLL 00 1

32.0000    0 1100 0011 0 0 0 0 LLLL HHHH 00 1
33.0000    1 0100 1001 1 0 0 0 LLHH HHLL 00 1
34.0000    0 0101 1010 0 0 0 0 LLHH HHLL 00 1
35.0000    0 0101 1010 1 0 0 0 HLHL LHLH 00 1
36.0000    0 0011 1100 0 0 0 0 HLHL LHLH 00 1

37.0000    0 0011 1100 1 0 0 0 HHLL LLHH 00 1
38.0000    1 0101 1010 0 0 0 0 HHLL LLHH 00 1
39.0000    0 1010 0101 1 0 0 0 LHLH HLHL 00 1
40.0000    1 0011 1100 0 0 0 0 LHLH HLHL 00 1
41.0000    1 0011 1100 1 0 0 0 LLHH HHLL 00 1

42.0000    1 1010 0101 0 0 0 0 LLHH HHLL 00 1
43.0000    1 1010 0101 1 0 0 0 HLHL LHLH 00 1
44.0000    1 1100 0011 0 0 0 0 HLHL LHLH 00 1
45.0000    1 1100 0011 1 0 0 0 HHLL LLHH 00 1
46.0000    1 0101 1010 0 0 0 0 HHLL LLHH 00 1

47.0000    1 0101 1010 1 0 0 0 LHLH HLHL 00 1
48.0000    1 1100 0011 0 1 0 0 LHLH HLHL 00 1
49.0000    1 1100 0011 1 1 0 0 HHLL HLHL 00 1
50.0000    1 1111 0000 0 1 1 1 1111 1111 00 1
51.0000    1 1111 0000 1 1 1 1 1111 1111 00 1

52.0000    1 1111 0000 1 1 0 0 HHHH HLHL 00 1
53.0000    0 0000 1111 0 1 1 1 1111 1111 00 1
54.0000    0 0000 1111 1 1 1 1 1111 1111 00 1
55.0000    0 0000 1111 1 1 0 0 HHHH HLHL 00 1
55.0100    *

55.0200    *
55.0300    * THE FIRST FOUR VECTORS ARE REPEATED SO ALL ERRORS ARE
55.0400    *   SAVED WITH NO ERRORS DETECTED ON A GOOD DEVICE.
56.0000     0 0000 1111 0 0 0 0 0000 0000 00 1
57.0000     0 0000 1111 1 0 0 0 HHHH LLLL 00 1
```

```
1                          0                 0
  TO                       1                 2
      24  1 2345 6789 0 1 2 3 4567 8901 23 4

58.0000   0 0000 1111 0 0 0 0 HHHH LLLL 00 1
59.0000   0 0000 1111 1 0 0 0 HHHH LLLL 00 1
59.0100  *THE FOLLOWING VECTORS CHECK DEVICE CAPABILITY OF
59.0200  *          RECEIVING DATA VIA BUS INPUT
59.0300  *

60.0000   0 0000 0000 0 0 0 1 LLLL 0000 00 1
61.0000   0 0000 0000 0 0 0 1 0000 HHHH 00 1
62.0000   0 0000 0000 0 0 0 1 1111 LLLL 00 1
63.0000   0 0000 0000 0 0 0 1 0000 HHHH 00 1
63.0100  *THE FIRST FOUR VECTORS ARE REPEATED SO ALL ERRORS ARE
63.0200  *     SAVED WITH NO ERRORS DETECTED ON A GOOD DEVICE
63.0300  *

64.0000   0 0000 0000 0 0 0 1 LLLL 0000 00 1
65.0000   0 0000 0000 0 0 0 1 0000 HHHH 00 1
66.0000   0 0000 0000 0 0 0 1 1111 LLLL 00 1
67.0000   0 0000 0000 0 0 0 1 0000 HHHH 00 1
```

DK0:P2915.PIN:NCT DATE: 06-FEB-78 TIME: 20:58:24

LINE NUMBER	SECTOR NUMBER	PIN NAME	OUT PIN OR COMMENT
1.0000	1WAIO	P1	RECEIVER LATCH ENABLE-NOT
2.0000	5WAIO	P2	RECEIVER OUTPUT 0
3.0000	9WAIO	P3	B0 INPUT
4.0000	13WAIO	P4	A0 INPUT
5.0000	17WAIO	P5	BUS I\O 0
6.0000	21WAIO	P6	GROUND 1
7.0000	25WAIO	P7	BUS I\O 1
8.0000	29WAIO	P8	A1 INPUT
9.0000	33WAIO	P9	B1 INPUT
10.0000	37WAIO	P10	RECEIVER OUTPUT 1
11.0000	41WAIO	P11	BUS ENABLE-NOT
12.0000	45WAIO	P12	OUTPUT ENABLE-NOT
13.0000	49WAIO	P13	SELECT A OR B INPUTS
14.0000	53WAIO	P14	RECEIVER OUTPUT 2
15.0000	57WAIO	P15	B2 INPUT
16.0000	61WAIO	P16	A2 INPUT
17.0000	2XAIO	P17	BUS I\O 2
18.0000	6XAIO	P18	GROUND 2
19.0000	10XAIO	P19	BUS I\O 3
20.0000	14XAIO	P20	A3 INPUT
21.0000	18XAIO	P21	B3 INPUT
22.0000	22XAIO	P22	RECEIVER OUTPUT 3
23.0000	26XAIO	P23	DRIVER CLOCK INPUT
24.0000	30XAIO	P24	POWER VCC INPUT

ii. Tektronix 3260 test for the 2916

The following pages contain the test program, pattern file, and pin assignment program for the 2916.

```
DK0:P2916A.EDT;WCT    DATE: 22-FEB-78    TIME: 13:48:42    PAGE  1

1.0100 *          THIS TEST IS FOR THE 2916 DEVICE
1.0200 *  WRITTEN BY L.W.ROLLER
1.0300 *  PIN ASSIGNMENT TABLE FOR THIS DEVICE IS P2916.PIN:WCT
1.0400 *  TEST PATTERN FILE NAME FOR THIS DEVICE IS P2916.PAT:WCT
1.0500 *   SOCKET CARD USED FOR THIS DEVICE IS S/N 2010
1.0600
1.0700 *        TABLE OF CONTENTS
1.0800 *  PART     DESCRIPTION OF CONTENTS
1.0900
1.1000 *     2     PINLISTS, ARRAYS, AND CONSTANTS
1.1100 *     3     FUNCTIONAL TESTS
1.1200 *   485     OUTPUT LEAKAGE CURRENT TESTS
1.1300 *    50     READ,SORT,AND PRINT FAILURES FROM FUNCTIONAL TEST

2.0100
2.0200    PINLIST CNT  = P1,P11,P23,P13
2.0300    PINLIST ADRS = P4,P3,P8,P9,P16,P15,P20,P21
2.0400    PINLIST INS1 = CNT,ADRS
2.0500    PINLIST BUS  = P5,P7,P17,P19
2.0510    PINLIST INS2 = CNT,ADRS,BUS
2.0600    PINLIST REC  = P2,P10,P14,P22
2.0700    PINLIST PAR  = P12
2.0800    PINLIST OUTS1 = BUS,REC,PAR
2.0810    PINLIST OUTS2 = REC,PAR
2.0900    PINLIST ALL  = P1,P2,P3,P4,P5,P7,P8,P9,P10,P11/
2.1000    P12,P13,P14,P15,P16,P17,P19,P20,P21,P22,P23
2.1100
2.1200 * THIS UNDERSOCKET BIT OPENS GROUND CONNECTION TO OUT PIN 12
2.1300
2.1500    SUBROUTINE EVS6(0),OVS6(0):MC3
2.1600    FUNCTION MVS6(V),IVS6(0):MC3
2.1700    SUBROUTINE CRDATE(V),CRTIME(V):TIME
2.1800    FUNCTION GETBIT(I,V,V,V):BARRAY
2.1900    SUBROUTINE BARRAY(I,V,V,V):BARRAY
2.2000    SUBROUTINE SREAD(P,V,V,V,V,I,V):SREAD
2.2100    IARRAY REP(85),PIN(10),C(70),D(70)
```

```
2.2200    ARRAY FF(70,10),V(50)
2.2300    RARRAY(RER,2,9,66)
2.2400    ARRAY VALUE(11,12)
2.2500
2.2600 *    ASSIGNMENTS ARE AS FOLLOWS
2.2700
2.2800 *    LUN   DATA OUTPUT
2.2900
2.3000 *      3      SELECTION QUERY
2.3100 *      4      TEST SUMMARY
2.3200 *      5      DATA ON A SPECIFIC PARAMETER
2.3300 *
2.3400 *           LABEL DATE AND TIME DATA IS TAKEN
2.3500 *
2.3600    PRINT <5> ERASE
2.3700    PRINT <5> CR,"DATE: "
2.3800    CRDATE(5)
2.3900    PRINT <5> CR,"TIME: "
2.4000    CRTIME(5)
2.4100    PRINT <5> CR
2.4200    PRINT <5> CR,CR,"THIS TEST IS FOR THE 2916 DEVICE",CR,CR

3.0100    INITIALIZE
3.0150    UNDERSOCKET #000001
3.0200    CONNECT INPUT TO GROUND ON P6
3.0300    CONNECT INPUT TO GROUND ON P18
3.0400    VS6 = 4.5V AT 95MA
3.0500    EVS6
3.0600    X = MVS6(10)
3.0700    Y = IVS6
3.0800    IF(5MA<Y<95MA) 3.13,3.13,3.09
3.0900    PRINT <4> "DEVICE DRAWS MORE THAN 95MA OF CURRENT"
3.1000    PRINT <4> CR,CR,"CHECK TO ENSURE DEVICE IS INSTALLED CORRECTLY",CR
3.1100    DVS6
3.1200    STOP
3.1300    IF(4.455V<X<4.545V)3.14,3.2,3.17
3.1400    PRINT <4> "SUPPLY VOLTAGE IS <4.455V",CR
3.1500    DVS6
```

```
3.1600    STOP
3.1700    PRINT <4> "SUPPLY VOLTAGE IS > 4.545V",CR
3.1800    DVS6
3.1900    STOP
3.2000    CONTINUE
3.2100    CYCLE = 500NS
3.2200    HICOMPARE = 200NS FOR 100NS
3.2300    LOCOMPARE = 200NS FOR 100NS
3.2400    CONNECT INPUT TO DRIVER ON INS1
3.2500    CONNECT OUTPUT TO COMPARATOR ON OUTS1
3.2600    HICOMPARE = 2.4V ON OUTS1
3.2700    HICOMPARE = 2.5V ON PAR
3.2800    LOCOMPARE = 0.4V ON OUTS1
3.2900    HIDRIVE = 2.0V ON INS1
3.3000    LODRIVE = 0.8V ON INS1
3.3100    LOAD DISK P2916 TO ALL WITH FI,CM
3.3200    FORCE INS1 WITH PATTERN
3.3300    COMPARE OUTS1 WITH PATTERN
3.3400    MASK OUTS1 WITH PATTERN
3.3500    MOVE REGISTER (63) TO ALL WITH FI,CM AND SAVE ERRORS
3.3510    H = 59
3.3520    K = 0
3.3530    A=1
3.3600    F=ERROR
3.3700    IF (NOT F)3.39
3.3800    GO TO 50.03
3.3900    PRINT <4> "PASSED FUNCTIONAL TEST PART 1 ",CR
3.4000    CONTINUE
3.4200    DISCONNECT OUTPUT FROM COMPARATOR ON BUS
3.4210    FORCE P11 WITH ONE
3.4300    CONNECT INPUT TO DRIVER ON BUS
3.4700    HIDRIVE = 2.0V ON BUS
3.4800    LODRIVE = 0.8V ON BUS
3.4900    LOAD DISK P2916 (64,71) TO ALL WITH FI,CM
3.5000    FORCE INS2 WITH PATTERN
3.5100    COMPARE OUTS2 WITH PATTERN
3.5200    MASK OUTS2 WITH PATTERN
3.5250    MASK BUS WITH ONE
```

```
3.5300   MOVE REGISTER (A) TO ALL WITH FI,CM AND SAVE ERRORS
3.5310   M = 4
3.5320   K = 43
3.5400   G=ERROR
3.5410   F = F+G
3.5500   IF (ODT 6)3.6
3.5600   GOTO 50.01
3.6000   PRINT <4> "PASSED FUNCTIONAL TEST PART 2",CR
3.7000   IF (F) 50.18

4.0100
4.0200 *   SETUP FOR OUTPUT LEAKAGE CURRENT ON OUTPUTS WHICH WERE HIGH
4.0300 *   IMPEDANCE STATE IN FUNCTIONAL TESTS
4.0400   DISCONNECT OUTPUT FROM COMPARATOR ON OUTS2
4.0410   DISCONNECT INPUT FROM DRIVER ON BUS
4.0500   VS6=5.5V AT 95MA
4.0600   X=4VS6(10)
4.0700   IF (5.445V<X<5.555V)4.1
4.0800   PRINT <4> CR,"** FAILED POWER SUPPLY VERIFICATION TEST **"
4.0900   STOP
4.1000   LOAD DISK P291A TO ALL WITH FI,CM
4.1100   HIDRIVE =2.0V ON INS1
4.1200   LODRIVE =0.8V ON INS1
4.1300   FORCE INS1 WITH PATTERN
4.1400   Z=9
4.1500   P=1
4.1600   CALL 5.01
4.1700   Z=15
4.1800   P=2
4.1900   CALL 5.01
4.2000   Z=21
4.2100   P=3
4.2200   CALL 5.01
4.2300   Z=27
4.2400   P=4
4.2500   CALL 5.01
4.2600   Z=29
4.2700   P=5
```

```
4.2800    CALL 5.01
4.2900    Z=46
4.3000    P=6
4.3100    CALL 5.01
4.3200    Z=47
4.3300    P=7
4.3400    CALL 5.01
4.3500    Z=50
4.3600    P=8
4.3700    CALL 5.01
4.3800    Z=51
4.3900    P=9
4.4000    CALL 5.01
4.4400    GOTO 6.02

5.0100 *  THE FOLLOWING STORES OUTPUT LEAKAGE CURRENTS ON BUS OUTPUTS
5.0200    V(P)=Z
5.0300    MOVE REGISTER (Z) TO ALL WITH FI,CM
5.0400    LOOP 5.11 I = 1,4
5.0500    SETUP TO MEASURE CURRENT ON BUS(I) FROM VS4=4.5V AT 500UA
5.0600    VALUE(P,I+8)=CURRENT
5.0700    VS4 = 2.4V AT 100UA
5.0800    VALUE(P,I+4)=CURRENT
5.0900    VS4=0.4V AT -300UA
5.1000    VALUE(P,I)=CURRENT
5.1100    UNSET TO MEASURE CURRENT ON BUS(I) FROM VS4
5.1200    RETURN
5.1300

6.0100 *   FOLLOWING PRINTS OUTPUT LEAKAGE CURRENTS AND DEFINES FAILURES
6.0200    PRINT <5> CR,"     OUTPUT LEAKAGE CURRENT TEST RESULTS",CR,CR
6.0300    PRINT <5> "BUS OUTPUTS",CR
6.0400    PRINT <5> "VECTOR# OUTPUT#    VO=0.4V          VO=2.4V          VO=4.5V",CR
6.0500    PRINT <5> "     LIMITS ARE =  200UA             50UA            100UA",CR
6.0600    P=0
6.0700    LOOP 6.29 P=1,9
6.0800    PRINT <5> CR,V(P):I2
6.0900    LOOP 6.28 I=1,4
```

```
6.1000    PRINT <5> "    ",(I-1):I1,"    ",VALUE(P,I)
6.1100    IF (-200UA<VALUE(P,I)<200UA) 6.15
6.1200    PRINT <5> " FAILED "
6.1300    B=1
6.1400    GOTO 6.16
6.1500    PRINT <5> "        "
6.1600    PRINT <5> VALUE(P,I+4)
6.1700    IF (-50UA<VALUE(P,I+4.01)<50UA) 6.21
6.1800    PRINT <5> " FAILED "
6.1900    B=1
6.2000    GOTO 6.22
6.2100    PRINT <5> "        "
6.2200    PRINT <5> VALUE(P,I+8)
6.2300    IF (-100US<VALUE(P,I+8)<100UA) 6.27
6.2400    PRINT <5> " FAILED "
6.2500    B=1
6.2600    GOTO 6.28
6.2700    PRINT <5> "        "
6.2800    PRINT <5> CR,"     "
6.2900    CONTINUE
6.3000    PRINT <4> CR,CR,CR,"SUMMARY OF TEST RESULTS",CR,CR
6.3100    PRINT <4> "*************************************************************",CR
6.3200    S=0
6.3300    IF (NOT F) 6.37
6.3400    PRINT <4> "*   FAILED FUNCTIONAL TESTS                                 *",CR
6.3500    S=1
6.3600    GOTO 6.38
6.3700    PRINT <4> "*   PASSED FUNCTIONAL TESTS                                 *",CR
6.3800    IF (NOT B) 6.42
6.3900    PRINT <4> "*   FAILED OUTPUT LEAKAGE TEST ON BUS OUTPUTS               *",CR
6.4000    S=1
6.4100    GOTO 6.43
6.4200    PRINT <4> "*   PASSED OUTPUT LEAKAGE TEST ON BUS OUTPUTS               *",CR
6.4300    PRINT <4> "*************************************************************",CR,CR
6.4400    IF (S EQ 0) 6.47
6.4500    DISPLAY 00,FAIL
6.4600    GOTO 6.48
6.4700    DISPLAY 00,PASS
6.4800    STOP
```

```
50.0100 *          SORT FAILING FUNCTIONAL TEST DATA
50.0200 *
50.0210    SREAD (OUTS2,0,0,5,H,HER,2)
50.0230    GOTO 50.06
50.0300    SREAD (OUTS1,1,9,5,H,HER,2)
50.0400    PRESET PIN(1)=5,7,17,19,2,10,14,22,12
50.0600    LOOP 50.17 J=1,H
50.0700    S=0
50.0800    LOOP 50.12 I=1,9
50.0900    IF (NOT GETBIT(HER,1,I,J)) 50.12
50.1000    S=S+1
50.1100    FF(A,S)=I
50.1200    CONTINUE
50.1300    IF (S EQ 0) 50.17
50.1400    C(A)=J+K
50.1500    D(A)=S
50.1600    A=A+1
50.1700    CONTINUE
50.1710    IF (K EQ 0) 3.0
50.1720    GOTO 3.7
50.1900    A=A-1
50.1900
50.2000    PRINT <5> "THE FOLLOWING FUNCTIONAL TESTS FAILED ",CR
50.2100    PRINT <5> "VECTOR NUMBER :  FAILING PINS",CR
50.2200    LOOP 50.26 J=1,A
50.2300    PRINT <5> CR,C(J):I,":  "
50.2400    LOOP 50.25 I=1,D(J)
50.2500    PRINT <5> PIN(FF(J,I)):I4
50.2600    CONTINUE
50.2700    PRINT <5> CR,"FAILED ",A:I," OUT OF 67 FUNCTIONAL TESTS",CR
50.2800    GOTO 4.01
```

```
DATE  22-FEB-7A      TIME  13:21      PATTERN FILE   P2916.PAT;WCT

 1                      0          0
   TO                   1          2
      21  12345 67890123456 78901

  0.0001  *
  0.0002  * THE FOLLOWING ARE THE DEVICE PIN NUMBERS
  0.0003  *
  0.0004  *          11111111 12222
  0.0005  *12345 78901234567 90123

  0.0006  *
  0.0007  * THE FOLLOWING ARE THE DEVICE PIN NAMES
  0.0008  *
  0.0009  *     9 8          8 8   D
  0.0010  *R    D U    0     D D   R

  0.0011  *LRBAS SARRRD RRAS SARRC
  0.0012  *E0000 1111E092222 3333P
  0.0013  *
  1.0000   00100 00100L00100 00100
  2.0000   0L10H H01L0L0L10H H01L1

  3.0000   0L10H HQ1L0L0L10H H01L0
  4.0000   0L11H H11L0H0L11H H01L0
  5.0000   0L10H H11L0H0L11H H11L0
  6.0000   0L11H H11L0L0L10H H01L0
  7.0000   0H11L L11H0L0L10H H01L1

  8.0000   1H11L L11H0L0L10H H01L1
  9.0000   1H111 111H1L0L101 101L1
 10.0000   0H11L L11H0L0L10H H01L1
 11.0000   0H11L L11H0L0L10H H01L0
 12.0000   0H11L L01H0L0L11H H01L0

 13.0000   0H11L H01L0L0H11L H01L1
 14.0000   1H11L H01L0L0H11L H01L1
 15.0000   1H111 101L1L0H111 101L1
 16.0000   0H11L H01L0L0H11L H01L1
 17.0000   0H11L H01L0L0H11L H01L0

 18.0000   0H10L H01L0H0H10L H11L0
 19.0000   0L10H H01L0H0L10H L11H1
 20.0000   1L10H H01L0H0L10H L11H1
 21.0000   1L101 101L1H0L101 111H1
 22.0000   0L10H H01L0H0L10H L11H1

 23.0000   0L10H H01L0H0L10H L11H0
 24.0000   0L01H H11L0H1L11H L11H0
 25.0000   0L01H L11H0H1H11L L11H1
 26.0000   1L01H L11H0H1H11L L11H1
```

```
1                       0         0
  TO                    1         2
      21   12345 67890123456 78901

27.0000    1L011 111H1H1H111 111H1

28.0000    1L111 111H1H1H111 111H1
29.0000    1L01H L11H0H1H11L L11H1
30.0000    1L11H L10H0H1H01L L10H1
31.0000    1L11H L10H0H1H01L L10H0
32.0000    1L11L H10H0H1H01H H10H1
33.0000    0H11L H10L0H1L01H H10L1
34.0000    1H01L H11L0H1L11H H11L1

35.0000    1H01L H11L0H1L11H H11L0
36.0000    1H01H L11L0H1L11L L11L1
37.0000    0L01H L11H0H1H11L L11H0
38.0000    1L01H L11H0L1H11L L10H0
39.0000    1L01H L11H0L1H11L H10H1

40.0000    1L10H L10H0L0H01L H01H0
41.0000    1L10H L10H0L0H01L H01H1
42.0000    0L01H L10H0L1H10L H01L0
43.0000    0L01H H10L0L1H10L L01H1
44.0000    1L10H H01L0H1H01L L01H0

45.0000    1L10L L01L0H1H01H L01H1
46.0000    1L101 101L1L0H101 101H0
47.0000    1L101 101L1L0H101 101H1
48.0000    0L10H H01L0L0L10H H01L1
49.0000    1L01H H10L0L1L01H H10L0

50.0000    1L011 110L1L1L011 110L0
51.0000    1L011 110L1L1L011 110L1
52.0000    0L10H H01L0L1L10H H01L0
53.0000    0H10L L01H0L1H10L L01H1
54.0000    1H01L L10H0L1H01L L10H0

55.0000    1H01H H10H0L1H01H H10H1
56.0000    1H01H H10H0L0H01H H10H0
57.0000    1H01L L10H0L0H01L L10H1
58.0000    1H01L L10H0H0H01L L01H0
59.0000    1H01L L10H0H0H01L H01H1

59.0100  *
59.0200  *
59.0300  *THE FIRST FOUR VECTORS ARE REPEATED SO ALL ERRORS ARE SAVED
59.0400  *  WITH NO ERRORS DETECTED ON A GOOD DEVICE.
59.0500  *
```

```
1                    0          0
  TO                 1          2
      21   12345 67890123456 78901
```

```
60.0000   00100 00100L00100 00100
61.0000   0L10H H01L0L0L10H H01L1
62.0000   0L10H H01L0L0L10H H01L0
63.0000   0L11H H11L0H0L11H H01L0
63.1000  *THE FOLLOWING VECTORS CHECK DEVICE CAPABILITY OF

63.2000  *       RECEIVING DATA VIA BUS INPUT
64.0000   0000H H0001000000H H0000
65.0000   0H000 000H1L0H000 000H0
66.0000   0L001 100L1L0L001 100L0
67.0000   0H000 000H1L0H000 000H0
67.0100  *
67.0200  *THE FIRST FOUR VECTORS ARE REPEATED SO ALL ERRORS ARE SAVED

67.0300  *    WITH NO ERRORS DETECTED ON A GOOD DEVICE
68.0000   0000H H0001000000H H0000
69.0000   0H000 000H1L0H000 000H0
70.0000   0L001 100L1L0L001 100L0
71.0000   0H000 000H1L0H000 000H0
```

DK0:P2916.PIN:WCT DATE: 06-FEB-78 TIME: 20:50:02

LINE NUMBER	SECTOR NUMBER	PIN NAME	DUT PIN OR COMMENT
1.0000	1WAIO	P1	RECEIVER LATCH ENABLE
2.0000	5WAIO	P2	R0
3.0000	9WAIO	P3	B0
4.0000	13WAIO	P4	A0
5.0000	17WAIO	P5	BUS0
6.0000	21WAIO	P6	GROUND 1
7.0000	25WAIO	P7	BUS1
8.0000	29WAIO	P8	A1
9.0000	33WAIO	P9	B1
10.0000	37WAIO	P10	R1
11.0000	41WAIO	P11	BUS ENABLE
12.0000	45WAIO	P12	ODD PARITY
13.0000	49WAIO	P13	SELECT
14.0000	53WAIO	P14	R2
15.0000	57WAIO	P15	B2
16.0000	61WAIO	P16	A2
17.0000	2XAIO	P17	BUS2
18.0000	6XAIO	P18	GROUND 2
19.0000	10XAIO	P19	BUS3
20.0000	14XAIO	P20	A3
21.0000	18XAIO	P21	B3
22.0000	22XAIO	P22	R3
23.0000	26XAIO	P23	DRIVER CLOCK
24.0000	30XAIO	P24	VCC

iii. Tektronix 3260 test for the 2917

The following pages contain the test program, pattern file, and pin assignment program for the 2917.

```
DK0:P2917.PDT;WCT     DATE: 22-FEB-78     TIME: 13:45:27     PAGE  1

1.0100 *          THIS TEST IS FOR THE 2917 DEVICE
1.0200 *   WRITTEN BY L.W.ROLLER
1.0300 *   PIN ASSIGNMENT TABLE FOR THIS DEVICE IS P2917.PIN;WCT
1.0400 *   TEST PATTERN FILE NAME FOR THIS DEVICE IS P2917.PAT;WCT
1.0450 *   SOCKET CARD USED FOR THIS DEVICE IS S/N 2011
1.0500
1.0600 *         TABLE OF CONTENTS
1.0700 *   PART     DESCRIPTION OF CONTENTS
1.0800
1.0900 *     2      PINLISTS, ARRAYS, AND CONSTANTS
1.1000 *     3      FUNCTIONAL TESTS
1.1100 *   4&5      OUTPUT LEAKAGE CURRENT TESTS
1.1200 *    50      SORT ERRORS FROM FUNCTIONAL TESTS AND PRINT SORTED DATA

2.0100
2.0200    PINLIST DCLK = P19
2.0300    PINLIST EN   = P1,P9,P11
2.0400    PINLIST ADRS = P3,P7,P13,P17
2.0500    PINLIST BUS  = P4,P6,P14,P16
2.0600    PINLIST REC  = P2,P8,P12,P18
2.0700    PINLIST PAR  = P10
2.0800    PINLIST OUTS1 = BUS,REC,PAR
2.0810    PINLIST OUTS2 = REC,PAR
2.0900    PINLIST ALL  = P1,P2,P3,P4,P6,P7,P8,P9,P10,P11,P12,P13/
2.1000    P14,P16,P17,P18,P19
2.1100    PINLIST INS1  = DCLK,EN,ADRS
2.1110    PINLIST INS2 = DCLK,EN,ADRS,BUS
2.1200    SUBROUTINE FVS6(0),OVS6(0):MC3
2.1300    FUNCTION MVS6(V),IVS6(0):MC3
2.1400    SUBROUTINE CRDATE(V),CRTIME(V):TIME
2.1500    FUNCTION GETBIT(I,V,V,V):BARRAY
2.1600    SUBROUTINE BARRAY(I,V,V,V):BARRAY
2.1700    SUBROUTINE SREAD(P,V,V,V,V,I,V):SREAD
2.1800    IARRAY BER(86),PIN(10),C(60),D(60)
2.1900    ARRAY FF(60,10),V(50)
2.2000    BARRAY(BER,2,9,52)
```

```
2.2100    ARRAY VALUE(11,12)
2.2200
2.2300 *    ASSIGNMENTS ARE AS FOLLOWS
2.2400
2.2500 *    LUN   DATA OUTPUT
2.2600
2.2700 *      3       SELECTION QUERY
2.2800 *      4       TEST SUMMARY
2.2900 *      5       DATA ON A SPECIFIC PARAMETER
2.3000 *
2.3100 *            LABEL DATE AND TIME DATA IS TAKEN
2.3200 *
2.3250    PRINT <5> ERASE
2.3300    PRINT <5> CR,"DATE: "
2.3400    CRDATE(5)
2.3500    PRINT <5> CR,"TIME: "
2.3600    CRTIME(5)
2.3700    PRINT <5> CR,CR,"THIS TEST IS FOR THE 2917 DEVICE",CR,CR

3.0100    INITIALIZE
3.0200    CONNECT INPUT TO GROUND ON P5
3.0300    CONNECT INPUT TO GROUND ON P15
3.0400    VS6 = 4.5V AT 95MA
3.0500    EVS6
3.0550    RG =300OA
3.0600    X = MVS6(10)
3.0700    Y = IVS6
3.0800    IF(5MA<Y<95MA) 3.13,3.13,3.09
3.0900    PRINT <4> "DEVICE DRAWS MORE THAN 95MA OF CURRENT"
3.1000    PRINT <4> CR,CR,"CHECK TO ENSURE DEVICE IS INSTALLED CORRECTLY",CR
3.1100    OVS6
3.1200    STOP
3.1300    IF(4.455V<X<4.545V)3.14,3.2,3.17
3.1400    PRINT <4> "SUPPLY VOLTAGE IS <4.455V",CR
3.1500    OVS6
3.1600    STOP
3.1700    PRINT <4> "SUPPLY VOLTAGE IS > 4.545V",CR
3.1800    OVS6
```

```
3.1900    STOP
3.2000    CONTINUE
3.2100    CYCLE = 500NS
3.2200    HICOMPARE = 200NS FOR 100NS
3.2300    LOCOMPARE = 200NS FOR 100NS
3.2400    CONNECT INPUT TO DRIVER ON INS1
3.2500    CONNECT OUTPUT TO COMPARATOR ON OUTS1
3.2600    HICOMPARE = 2.4V ON OUTS1
3.2700    HICOMPARE = 2.5V ON PAR
3.2800    LOCOMPARE = 0.4V ON OUTS1
3.2900    HIDRIVE = 2.0V ON INS1
3.3000    LODRIVE = 0.8V ON INS1
3.3100    LOAD DISK P2917 TO ALL WITH FI,CM
3.3200    FORCE INS1 WITH PATTERN
3.3300    COMPARE OUTS1 WITH PATTERN
3.3400    MASK OUTS1 WITH PATTERN
3.3500    MOVE REGISTER (52) TO ALL WITH FI,CM AND SAVE ERRORS
3.3510    M = 4R
3.3520    K = 0
3.3530    A = 1
3.3600    F=ERROR
3.3610    CLEAR ERROR
3.3700    IF (NOT F)3.4
3.3900    GO TO 50.03
3.4000    PRINT <4> "PASSED FUNCTIONAL TEST PART 1 ",CR
3.4100    CONTINUE
3.4300    DISCONNECT OUTPUT FROM COMPARATOR ON BUS
3.4305    HIDRIVE=2.4V ON P9
3.4310    FORCE P9 WITH ONE
3.4400    CONNECT INPUT TO DRIVER ON BUS
3.4800    HIDRIVE = 2.0V ON BUS
3.4900    LODRIVE = 0.8V ON BUS
3.5000    LOAD DISK P2917 (53,60) TO ALL WITH FI,CM
3.5100    FORCE INS2 WITH PATTERN
3.5150    INHIBIT INS2 WITH PATTERN
3.5200    COMPARE OUTS2 WITH PATTERN
3.5250    MASK BUS WITH ONE
3.5300    MASK OUTS2 WITH PATTERN
```

```
3.5310    CLEAR ERROR
3.5400    MOVE REGISTER (A) TO ALL WITH FI,CM AND SAVE ERRORS
3.5410    H = 4
3.5420    K = 52
3.5500    G=ERROR
3.5510    F = F+G
3.5600    IF (NOT G)3.6
3.5610    GOTO 50.01
3.6000    PRINT <4> "PASSED FUNCTIONAL TEST PART 2",CR
3.7000    IF(F)50.18

4.0010 *    FOLLOWING PERFORMS OUTPUT LEAKAGE CURRENT TESTS ON
4.0020 *    OUTPUTS WHICH WERE HIGH IMPEDANCE STATE IN THE FUNCTION TESTS
4.0030
4.0100    DISCONNECT OUTPUT FROM COMPARATOR ON OUTS1
4.0110    DISCONNECT INPUT FROM DRIVER ON INS2
4.0200    VS6=5.5V AT 95MA
4.0300    X=MVS6(10)
4.0400    IF (5.445V<X<5.555V)4.07
4.0500    PRINT <4> CR,"**FAILED POWER SUPPLY VERIFICATION TEST**"
4.0600    STOP
4.0700    HIDRIVE =2.0V ON INS1
4.0800    LODRIVE = 0.8V ON INS1
4.0900    LOAD DISK P2917 TO ALL WITH FI,CM
4.1000    FORCE INS1 WITH PATTERN
4.1100    Z=9
4.1200    P=1
4.1300    CALL 5.01
4.1400    Z=10
4.1500    P=2
4.1600    CALL 5.01
4.1700    P=11
4.1800    CALL 5.29
4.1900    Z=16
4.2000    P=3
4.2100    CALL 5.01
4.2200    Z=17
4.2300    P=4
```

```
4.2400    CALL 5.01
4.2500    P=12
4.2600    CALL 5.29
4.2700    Z=23
4.2800    P=5
4.2900    CALL 5.01
4.3000    Z=24
4.3100    P=6
4.3200    CALL 5.01
4.3300    P=13
4.3400    CALL 5.29
4.3500    Z=30
4.3600    P=7
4.3700    CALL 5.01
4.3800    Z=31
4.3900    P=8
4.4000    CALL 5.01
4.4100    Z=43
4.4200    P=9
4.4300    CALL 5.01
4.4400    P=14
4.4500    CALL 5.29
4.4600    Z=44
4.4700    P=10
4.4800    CALL 5.01
4.4900    P=15
4.5000    CALL 5.29
4.5100    Z=47
4.5200    P=16
4.5300    CALL 5.29
4.5400    Z=48
4.5500    P=17
4.5600    CALL 5.29
4.5700    GOTO 6.01

5.0010 *   OUTPUT LEAKAGE CURRENT MEASUREMENTS WITH CURRENT RANGE STEPPED
5.0020 *   DOWN TO OBTAIN BETTER ACCURACY MEASUREMENTS AND RESOLUTION
5.0030
```

```
5.0100 *  THE FOLLOWING STORES OUTPUT LEAKAGE CURRENTS ON BUS OUTPUTS
5.0200    V(P)=Z
5.0300    MOVE REGISTER (Z) TO ALL WITH FT,CM
5.0400    LOOP 5.26 I = 1,4
5.0450    RG = 999UA
5.0500    SETUP TO MEASURE CURRENT ON BUS(I) FROM VS4=4.5V AT RG
5.0600    VALUE(P,I+8)=CURRENT
5.0650    UNSET TO MEASURE CURRENT ON BUS(I) FROM VS4
5.0700    IF (-RG/10 <VALUE(P,I+8)< RG/10) 5.08,5.12
5.0800    IF (RG LT 98V) 5.12
5.0900    RG = RG/10
5.1100    GOTO 5.05
5.1200    RG = 99UA
5.1300    SETUP TO MEASURE CURRENT ON BUS(I) FROM VS4=2.4V AT RG
5.1400    VALUE(P,I+4)=CURRENT
5.1450    UNSET TO MEASURE CURRENT ON BUS(I) FROM VS4
5.1500    IF (-RG/10 <VALUE(P,I+4) < RG/10) 5.16, 5.19
5.1600    IF (RG LT 98V) 5.19
5.1700    RG = RG/10
5.1800    GOTO 5.13
5.1900    RG = 999UA
5.2000    SETUP TO MEASURE CURRENT ON BUS(I) FROM VS4=0.4V AT RG
5.2100    VALUE(P,I)=CURRENT
5.2150    UNSET TO MEASURE CURRENT ON BUS(I) FROM VS4
5.2200    IF (-RG/10 <VALUE(P,I)< RG/10) 5.23,5.26
5.2300    IF (RG LT 98V) 5.26
5.2400    RG = RG/10
5.2500    GOTO 5.2
5.2600    CONTINUE
5.2700    RETURN
5.2800
5.2900 *  THE FOLLOWING STORES OUTPUT LEAKAGE CURRENTS ON REC OUTPUTS
5.3000
5.3100    V(P)=Z
5.3200    LOOP 5.47 I = 1,4
5.3250    RG = 99UA
5.3300    SETUP TO MEASURE CURRENT ON REC(I) FROM VS4=2.4V AT RG
5.3400    VALUE(P,I+4)=CURRENT
```

```
5.3450   UNSET TO MEASURE CURRENT ON REC(I) FROM VS4
5.3500   IF (-RG/10 <VALUE(P,I+4)< RG/10) 5.36,5.4
5.3600   IF (RG LT 98V) 5.4
5.3700   RG = RG/10
5.3900   GOTO 5.33
5.4000   RG = 99UA
5.4100   SETUP TO MEASURE CURRENT ON REC(I) FROM VS4=0.4V AT RG
5.4200   VALUE(P,I)=CURRENT
5.4250   UNSET TO MEASURE CURRENT ON REC(I) FROM VS4
5.4300   IF (-RG/10 <VALUE(P,I)< RG/10) 5.44,5.47
5.4400   IF (RG LT 98V) 5.47
5.4500   RG = RG/10
5.4600   GOTO 5.41
5.4700   CONTINUE
5.4800   RETURN

6.0010 *   FOLLOWING PRINTS OUTPUT LEAKAGE CURRENTS AND DEFINES FAILURES
6.0100   PRINT <5> CR,CR,"OUTPUT LEAKAGE CURRENT TEST RESULTS",CR,CR
6.0200   PRINT <5> "   BUS OUTPUT RESULTS",CR
6.0300   PRINT <5> "   VECTOR #   OUTPUT #   VO=0.4V          VO=2.4V          VO=4.5V",CR
6.0320   B=0
6.0350   PRINT <5> "              LIMITS ARE =  200UA            50UA             100UA"
6.0400   LOOP 6.2 P=1,10
6.0500   PRINT <5> CR,"     ",V(P):I2
6.0600   LOOP 6.19 I=1,4
6.0700   PRINT <5> "     ",(I-1):I1,"       ",VALUE(P,I)
6.0800   IF (-200UA<VALUE(P,I)<200UA) 6.105
6.0900   PRINT <5> " FAILED "
6.1000   B=1
6.1010   GOTO 6.11
6.1050   PRINT <5> "          "
6.1100   PRINT <5> VALUE(P,I+4)
6.1200   IF (-50UA<VALUE(P,I+4.01)<50UA) 6.145
6.1300   PRINT <5> " FAILED"
6.1400   B=B+1
6.1410   GOTO 6.15
6.1450   PRINT <5> "          "
6.1500   PRINT <5> VALUE(P,I+8)
```

```
6.1600   IF (-100US<VALUE(P,I+8)<100UA) 6.19
6.1700   PRINT <5> " FAILED"
6.1800   R=1
6.1900   PRINT <5> CR,"          "
6.2000   CONTINUE
6.2100   PRINT <5> CR,CR,"  RECEIVER OUTPUT RESULTS",CR
6.2200   PRINT <5> "   VECTOR#   OUTPUT#      VO=0.4V            VO=2.4V",CR
6.2250   PRINT <5> "          LIMITS ARE =      20UA               20UA"
6.2300   LOOP 6.35 P=11,17
6.2400   PRINT <5> CR,"     ",V(P):I2
6.2500   LOOP 6.34 I=1,4
6.2600   PRINT <5> "    ",(I-1):I1,"      ",VALUE(P,I)
6.2700   IF (-20UA<VALUE(P,I)<20UA) 6.295
6.2800   PRINT <5> " FAILED "
6.2900   R=1
6.2910   GOTO 6.3
6.2950   PRINT <5> "          "
6.3000   PRINT <5> "  ",VALUE(P,I+4)
6.3100   IF (-20UA<VALUE(P,I+4)<20UA ) 6.34
6.3200   PRINT <5> " FAILED"
6.3300   R=1
6.3400   PRINT <5> CR,"          "
6.3500   CONTINUE
6.3600   PRINT <4> CR,CR,CR,"SUMMARY OF TEST RESULTS",CR,CR
6.3650   PRINT <4> "**************************************************",CR
6.3680   S=0
6.3700   IF (NOT F) 6.4
6.3800   PRINT <4> "*   FAILED FUNCTIONAL TESTS                    *",CR
6.3850   S=1
6.3900   GOTO 6.41
6.4000   PRINT <4> "*   PASSED FUNCTIONAL TESTS                    *",CR
6.4100   IF (NOT B) 6.44
6.4200   PRINT <4> "*   FAILED OUTPUT LEAKAGE TEST ON BUS OUTPUTS  *",CR
6.4250   S=1
6.4300   GOTO 6.45
6.4400   PRINT <4> "*   PASSED OUTPUT LEAKAGE TEST ON BUS OUTPUTS  *",CR
6.4500   IF (NOT R) 6.48
6.4600   PRINT <4> "*   FAILED OUTPUT LEAKAGE TEST ON RECEIVER OUTPUTS  *",CR
```

```
6.4650    S=1
6.4700    GOTO 6.485
6.4800    PRINT <4> "*   PASSED OUTPUT LEAKAGE TEST ON RECEIVER OUTPUTS   *",CR
6.4850    PRINT <4> "*****************************************************",CR,CR
6.4855    IF (S EQ 0) 6.489
6.4856    DISPLAY 00,FAIL
6.4857    GOTO 6.49
6.4890    DISPLAY 00,PASS
6.4900    STOP

50.0100 *          SORT FAILING FUNCTIONAL TEST DATA
50.0200 *
50.0210   SREAD (OUTS2,9,0,5,H,HER,2)
50.0230   GOTO 50.06
50.0300   SREAD (OUTS1,1,9,5,H,HER,2)
50.0400   PRESET PIN(1)=4,6,14,16,2,8,12,18,10
50.0600   LOOP 50.17 J=1,H
50.0700   S=0
50.0800   LOOP 50.12 I=1,9
50.0900   IF (NOT GETBIT(HER,1,I,J)) 50.12
50.1000   S=S+1
50.1100   FF(A,S)=I
50.1200   CONTINUE
50.1300   IF (S EQ 0) 50.17
50.1400   C(A)=J+K
50.1500   D(A)=S
50.1600   A=A+1
50.1700   CONTINUE
50.1710   IF (K EQ 0) 5.41
50.1720   GOTO 3.7
50.1800   A=A-1
50.1900
50.2100   PRINT <5> "THE FOLLOWING FUNCTIONAL TESTS FAILED ",CR
50.2200   PRINT <5> "VECTOR NUMBER :  FAILING PINS",CR
50.2300   LOOP 50.27 J=1,A
50.2400   PRINT <5> CR,C(J):I,":  "
50.2500   LOOP 50.26 I=1,D(J)
50.2600   PRINT <5> PIN(FF(J,I)):I4
```

```
50.2700  CONTINUE
50.2750  PRINT <5> CR,CR,"   FAILED ",A:I," OUT OF 56 FUNCTIONAL TESTS",CR,CR
50.2800  GOTO 4.01
```

```
DATE  22-FEB-79      TIME  13:23      PATTERN FILE   P2917.PAT;WCT

1                      0
  TO                   1
       17  1234 567890123 4567

 0.0001  *
 0.0002  * THE FOLLOWING ARE THE DEVICE PIN NUMBERS
 0.0003  *
 0.0004  *          11111 1111
 0.0005  *1234 678901234 6789

 0.0007  * THE FOLLOWING ARE THE DEVICE PIN NAMES
 0.0008  *   R R         R R  D
 0.0009  *R  U U   D     U U  R
 0.0010  *LRAS SARBDDRAS SARC
 0.0011  *F000 111EDE222 333P

 1.0000   0000 0000L0000 0000
 2.0000   0L0H H0L0L0L0H H0L1
 3.0000   0L0H H0L0L0L0H H0L0
 4.0000   0L1H H1L0H0L1H H0L0
 5.0000   0L0H H1L0H0L1H H1L0

 6.0000   0L1H H1L0L0L0H H0L0
 7.0000   0H1L L1H0L0L0H H0L1
 8.0000   1H1L L1H0L0L0H H0L1
 9.0000   1H11 11H1L0L01 10L1
10.0000   1111 1111L1101 1011

11.0000   0H1L L1H0L0L0H H0L1
12.0000   0H1L L1H0L0L0H H0L0
13.0000   0H1L L0H0L0L1H H0L0
14.0000   0H1L H0L0L0H1L H0L1
15.0000   1H1L H0L0L0H1L H0L1

16.0000   1H11 10L1L0H11 10L1
17.0000   1111 1011L1111 1011
18.0000   0H1L H0L0L0H1L H0L1
19.0000   0H1L H0L0L0H1L H0L0
20.0000   0H0L H0L0H0H0L H1L0

21.0000   0L0H H0L0H0L0H L1H1
22.0000   1L0H H0L0H0L0H L1H1
23.0000   1L01 10L1H0L01 11H1
24.0000   1101 1011H1101 1111
25.0000   0L0H H0L0H0L0H L1H1

26.0000   0L0H H0L0H0L0H L1H1
27.0000   0L0H H1L0H0L1H L1H0
28.0000   0L0H L1H0H0H1L L1H1
29.0000   1L0H L1H0H0H1L L1H1
```

```
1                   0
  TO                1
      17  1234 567890123 4567

30.0000   1L01 11H1H0H11 1141

31.0000   1L11 11H1H0H11 11H1
32.0000   1L0H L1H0H0H1L L1H1
33.0000   1L1H L0H0H0H0L L0H1
34.0000   1L1H L0H0H0H0L L0H0
35.0000   1L1L H0H0H0H0H H0H1
36.0000   0H1L H0L0H0L0H H0L1
37.0000   1H0L H1L0H0L1H H1L1

38.0000   1H0L H1L0H0L1H H1L0
39.0000   1H0H L1L0H0L1L L1L1
40.0000   0L0H L1H0H0H1L L1H0
41.0000   1L0H L1H0L0H1L L0H0
42.0000   1L0H L1H0L0H1L H0H1

43.0000   1101 1011H1101 1010
44.0000   1101 1011H1101 1011
45.0000   0L1H H1L0L0L1H H1L0
46.0000   0H1L L1H0L0H1L L1H1
47.0000   011L L110L111L L110

48.0000   011L L110L111L L111
48.0200   *
48.0300   *
48.0400   * THE FIRST FOUR VECTORS ARE REPEATED SO ALL ERRORS ARE
48.0500   *   SAVED WITH NO ERRORS DETECTED ON A GOOD DEVICE.

49.0000   0000 0000L0000 0000
50.0000   0L0H H0L0L0L0H H0L1
51.0000   0L0H H0L0L0L0H H0L0
52.0000   0L1H H1L0H0L1H H0L0
52.0100   *THE FOLLOWING VECTORS CHECK DEVICE CAPABILITY OF

52.0200   *       RECEIVING DATA VIA BUS INPUT
53.0000   000H H0010000H H000
54.0000   0H00 00H1L0H00 00H0
55.0000   0L01 10L1L0L01 10L0
56.0000   0H00 00H1L0H00 00H0

56.0100   *
56.0200   *THE FIRST FOUR VECTORS ARE REPEATED SO ALL ERRORS ARE
56.0300   *  SAVED WITH NO ERRORS DETECTED ON A GOOD DEVICE
57.0000   000H H0010000H H000
58.0000   0H00 00H1L0H00 00H0

59.0000   0L01 10L1L0L01 10L0
60.0000   0H00 00H1L0H00 00H0
```

DK0:P2917.PIN:WCT DATE: 06-FEB-78 TIME: 20:50:14

LINE NUMBER	SECTOR NUMBER	PIN NAME	OUT PIN OR COMMENT
1.0000	1WAIO	P1	RECEIVER LATCH ENABLE
2.0000	5WAIO	P2	R0
3.0000	9WAIO	P3	A0
4.0000	13WAIO	P4	BUS0
5.0000	17WAIO	P5	GROUND 1
6.0000	21WAIO	P6	BUS1
7.0000	25WAIO	P7	A1
8.0000	29WAIO	P8	R1
9.0000	33WAIO	P9	BUS ENABLE
10.0000	37WAIO	P10	ODD PARITY
11.0000	41WAIO	P11	OUTPUT ENABLE
12.0000	45WAIO	P12	R2
13.0000	49WAIO	P13	A2
14.0000	53WAIO	P14	BUS2
15.0000	57WAIO	P15	GROUND 2
16.0000	61WAIO	P16	BUS3
17.0000	2XAIO	P17	A3
18.0000	6XAIO	P18	R3
19.0000	10XAIO	P19	DRIVER CLOCK
20.0000	14XAIO	P20	VCC

iv. Socket card wiring lists

The following pages contain the wiring lists for socket cards S/N 2010 and S/N 2011. The former is used for testing the 2915 and 2916 and the latter for the 2917.

SOCKET CARD S/N 2010 WIRING LIST

DUT PIN	To	I/O PIN	SOCKET CARD I/O JUMPERS	
1		1	1 W I	1 W O
2		5	2 X I	2 X O
3		9	5 W I	5 W O
4		13	6 X I	6 X O
5		17	9 W I	9 W O
6		21	10 X I	10 X O
7		25	13 W I	13 W O
8		29	14 X I	14 X O
9		33	17 W I	17 W O
10		37	18 X I	18 X O
11		41	21 W I	21 W O
12		45	22 X I	22 X O
13		49	25 W I	25 W O
14		53	26 X I	26 X O
15		57	29 W I	29 W O
16		61	30 X I	30 X O
17		2	33 W I	33 W O
18		6	37 W I	37 W O
19		10	40 Z I	40 Z O
20		14	41 W I	41 W O
21		18	45 W I	45 W O
22		22	49 W I	49 W O
23		26	52 Z I	52 Z O
24		30	53 W I	53 W O

57 W I	57 W O
61 W I	61 W O

UNDER SOCKET CONNECTOR WIRING

C A 7	TO	D U T 24	C B 25	TO	C A 13
C A 8		D U T 24	C A 13		C A 14
C A 9		RING gnd	C A 11		C A 12
C A 10		RING gnd	* D U T 6		RING gnd
C B 25		RING gnd	* D U T 18		RING gnd

* 2915 and 2916 Devices Only

SOCKET CARD S/N 2011

WIRING LIST

DUT PIN	to	I/O PIN	SOCKET CARD	to	I/O JUMPERS
1		1	1 WI		1 WO
2		5	5 WI		5 WO
3		9	9 WI		9 WO
4		13	13 WI		13 WO
5		17	17 WI		17 WO
6		21	21 WI		21 WO
7		25	25 WI		25 WO
8		29	29 WI		29 WO
9		33	33 WI		33 WO
10		37	37 WI		37 WO
11		41	41 WI		41 WO
12		45	45 WI		45 WO
13		49	49 WI		49 WO
14		53	53 WI		53 WO
15		57	57 WI		57 WO
16		61	61 WI		61 WO
17		2	2 XI		2 XO
18		6	6 XI		6 XO
19		10	10 XI		10 XO
20		14	14 XI		14 XO

UNDER SOCKET CONNECTOR TO DUT PIN AND GROUND

CA7	TO	DUT 20
CA8		DUT 20
CA9		Ring Gnd
CA10		Ring Gnd
CB25		Ring Gnd

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